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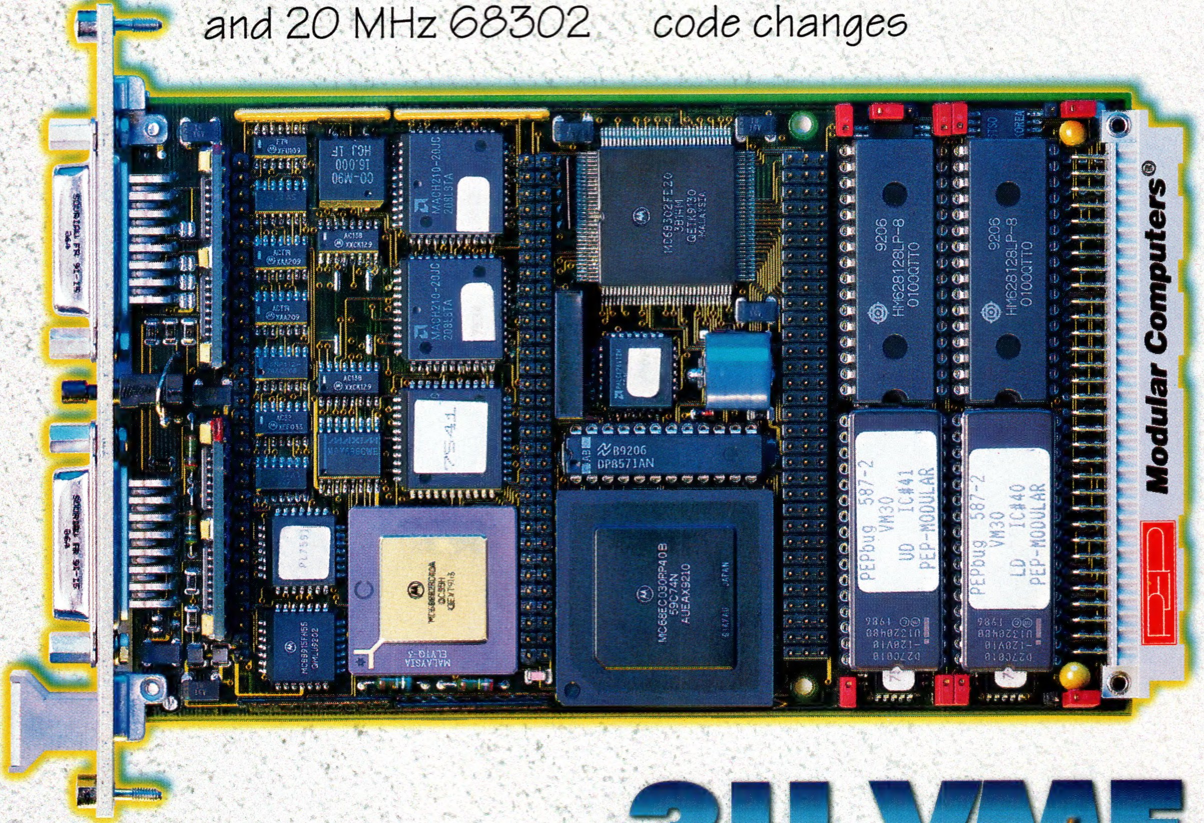
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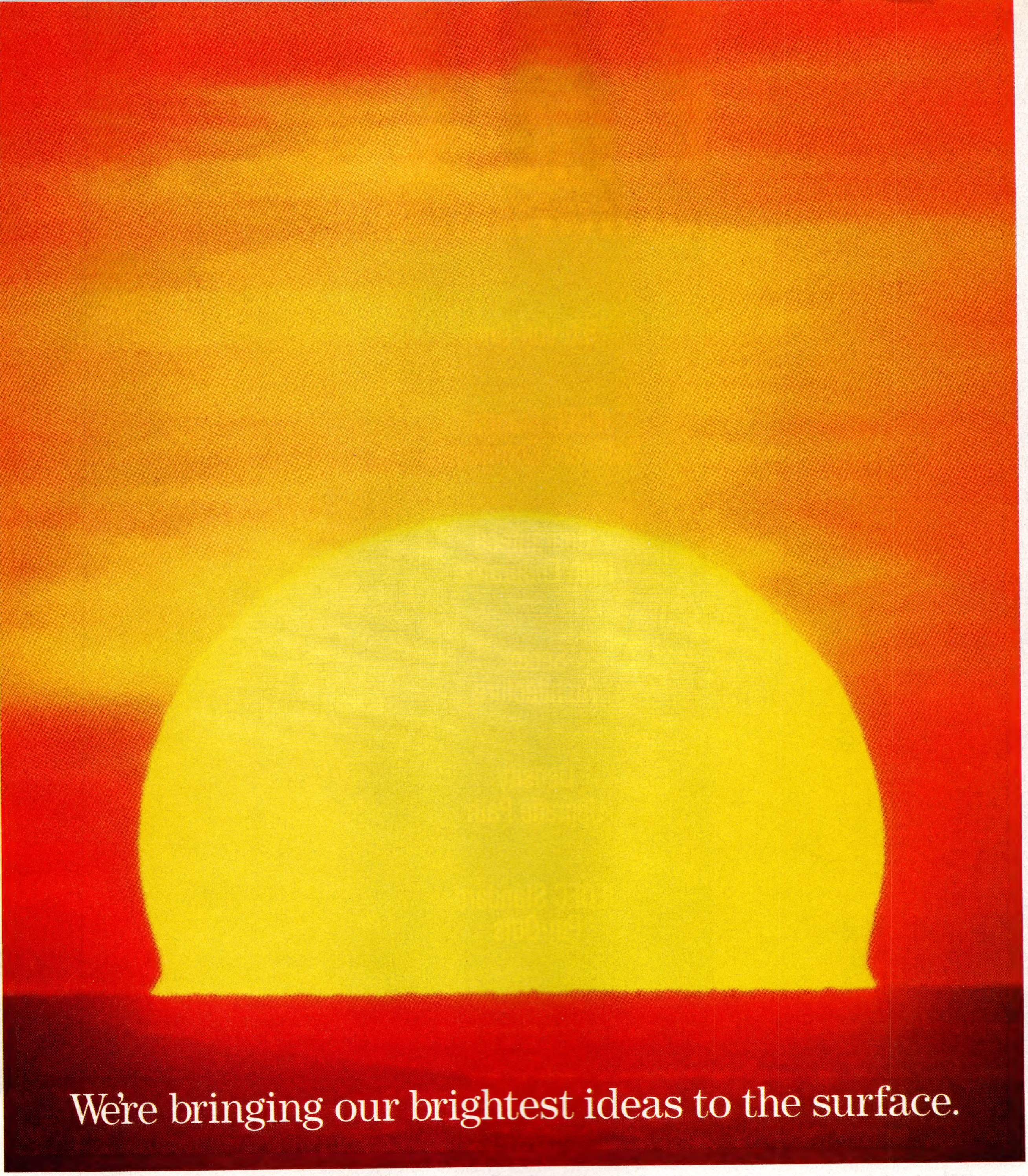

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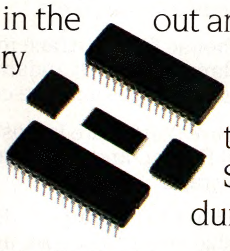

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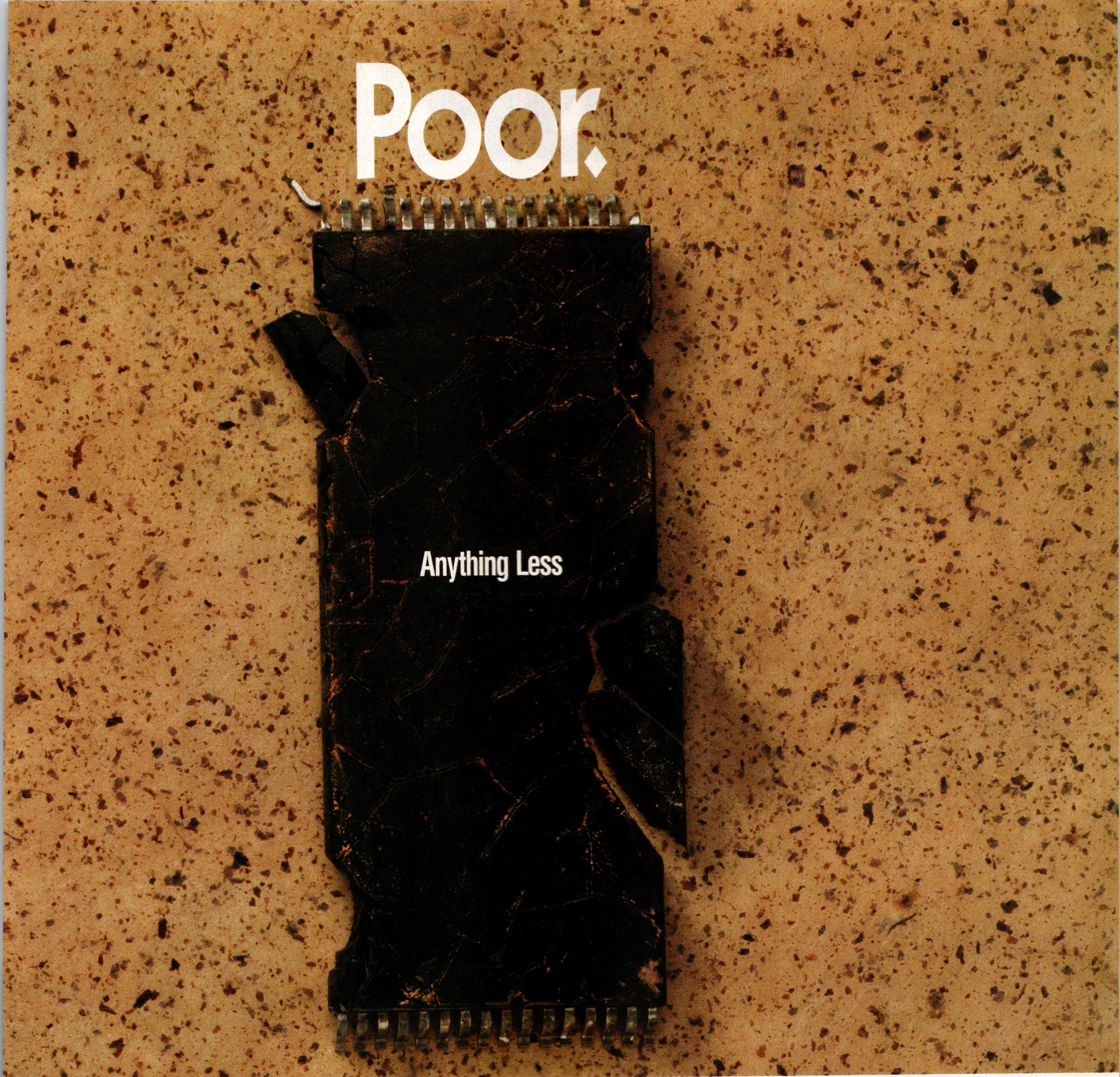

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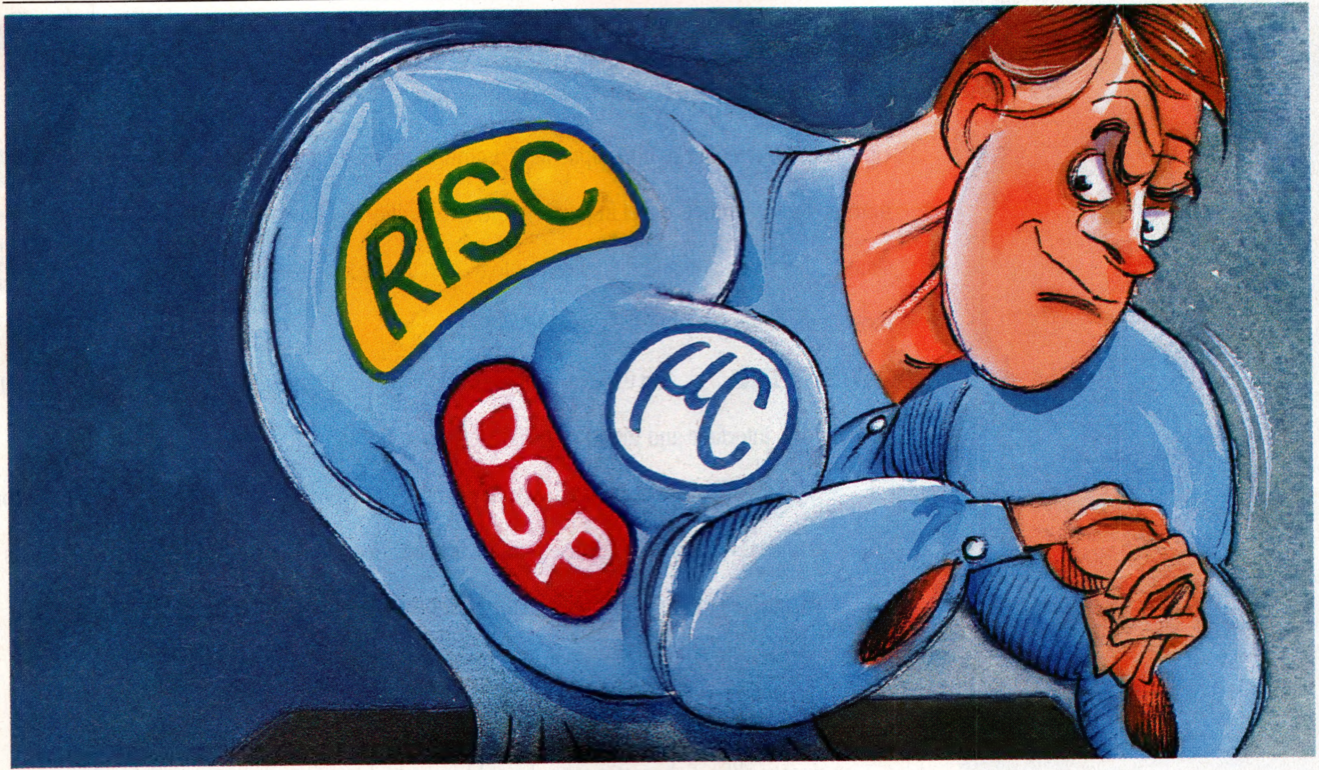

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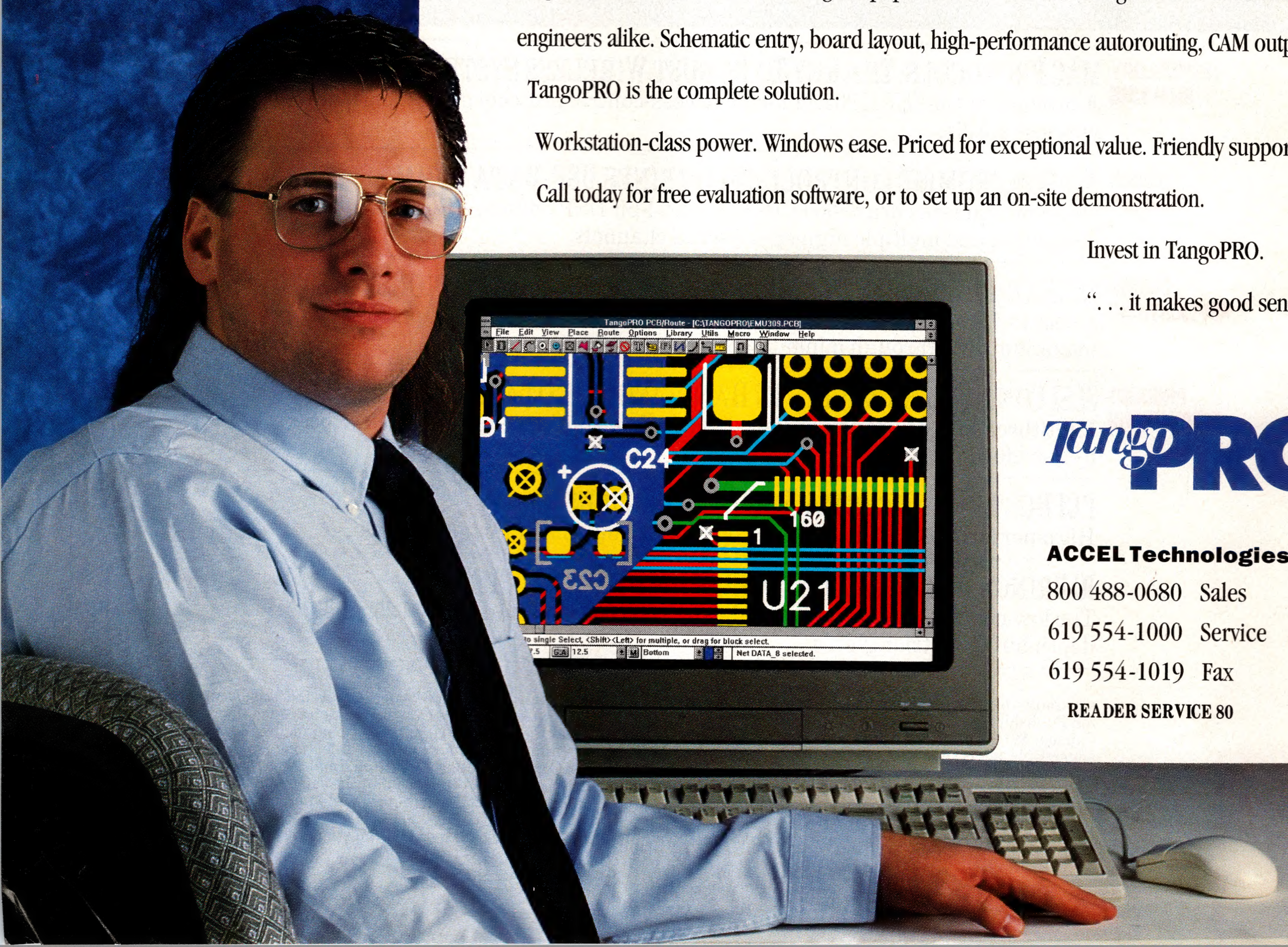
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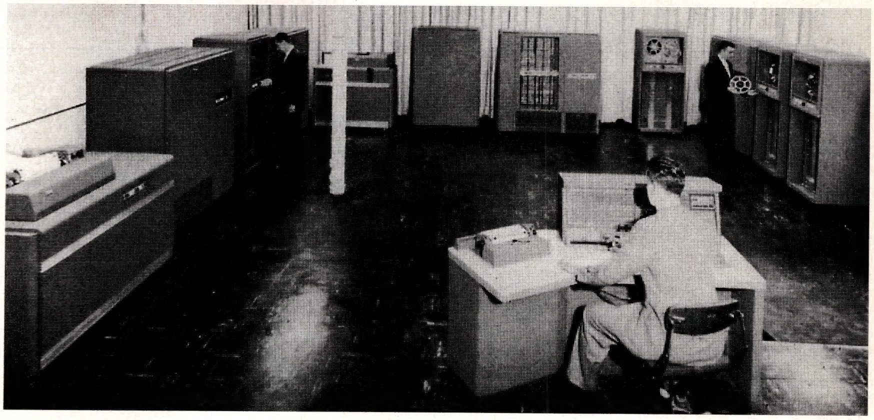
ELECTRONIC DESIGN 40 YEARS AGO

Business Data Computer



More than 10 million operations per hour can be performed by the Type 702 electronic commercial data processing machine shown here. Manufactured by International Business Machines Corp., 590 Madison Avenue, New York 22, N.Y., the computer is designed to handle the complex logic of business problems which involves a wide variety of input and output data, and many exceptions to the rules for handling them.*(Electronic Design, June 1954, p. 5.)*

The 702 was just one of the 700-series systems that IBM developed in the 1950s on its way to the top of the heap by the end of the decade. By the way, note the performance of this vacuum-tube-based computer: 10 million operations per hour. Today, we talk in millions of operations per second.—SS

Tiny Radio for Civil Defense

A five-ounce radio receiver, which can be worn like a hearing aid, has been developed for use in civil defense. Described as an experimental model, it is tuned to a single broadcast frequency, 1260kc, which is one of two channels to be used by radio stations in broadcasting civil defense instructions during emergency periods. Employing a transistor and a double-based germanium diode, the receiver is capable of continuous operation for more than a month without requiring replacement of its two small batteries. Developed by W.F. Chow and J.J. Suran of the General Electric Company, Syracuse, N.Y., the unit has a hearing-aid type earphone.*(Electronic Design, June 1954, p. 5.)*

J.J. "Jerry" Suran now teaches in the College of Engineering and the Graduate School of Management at the University of California at Davis after a long career in semiconductors with General Electric. He's also well-known for his work with the International Solid State Circuits Conference, and as a member of the IEEE Spectrum Editorial Board. He recalls that this radio was designed as a superregenerative receiver because of the lack of high-frequency transistors, and points out that the double-base diode later became the unijunction transistor, which enjoyed a long product life with many applications. —SS

Battery Slide Rule Selector

This circular slide-rule-type application guide selects the proper chargeable battery for a particular ampere-hour requirement. Plastic-covered, the 4" x 5-1/2" guide lists all of this firm's nickel-silver alkaline batteries from 1/2 to 100 ampere-hours capacity. On the back of the guide, typical characteristic curves for the units are shown. Yardney Electric Corp., 105 Chambers St., New York 7, N.Y.*(Electronic Design, June 1954, p. 70.)*

It seems that manufacturers have stopped offering promotional gadgets like this. At one time, engineers could circle bingo numbers in magazines and fill their desk drawers with specialized slide-rule selectors, nomographs, and the like, all offered by manufacturers to support sales of their parts. Perhaps it was the demise of the slide rule itself that caused the decline in the popularity of such items.—SS

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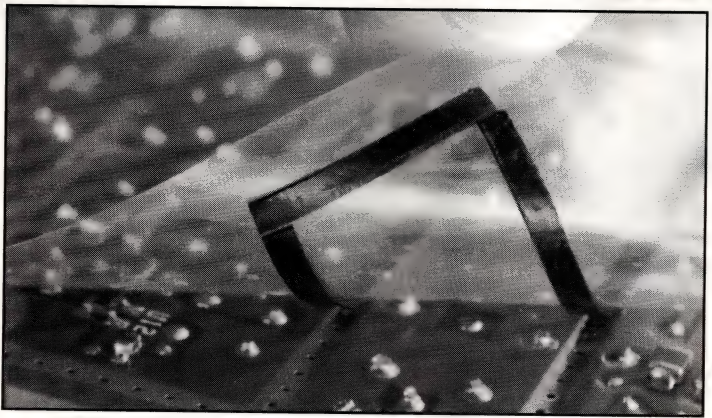

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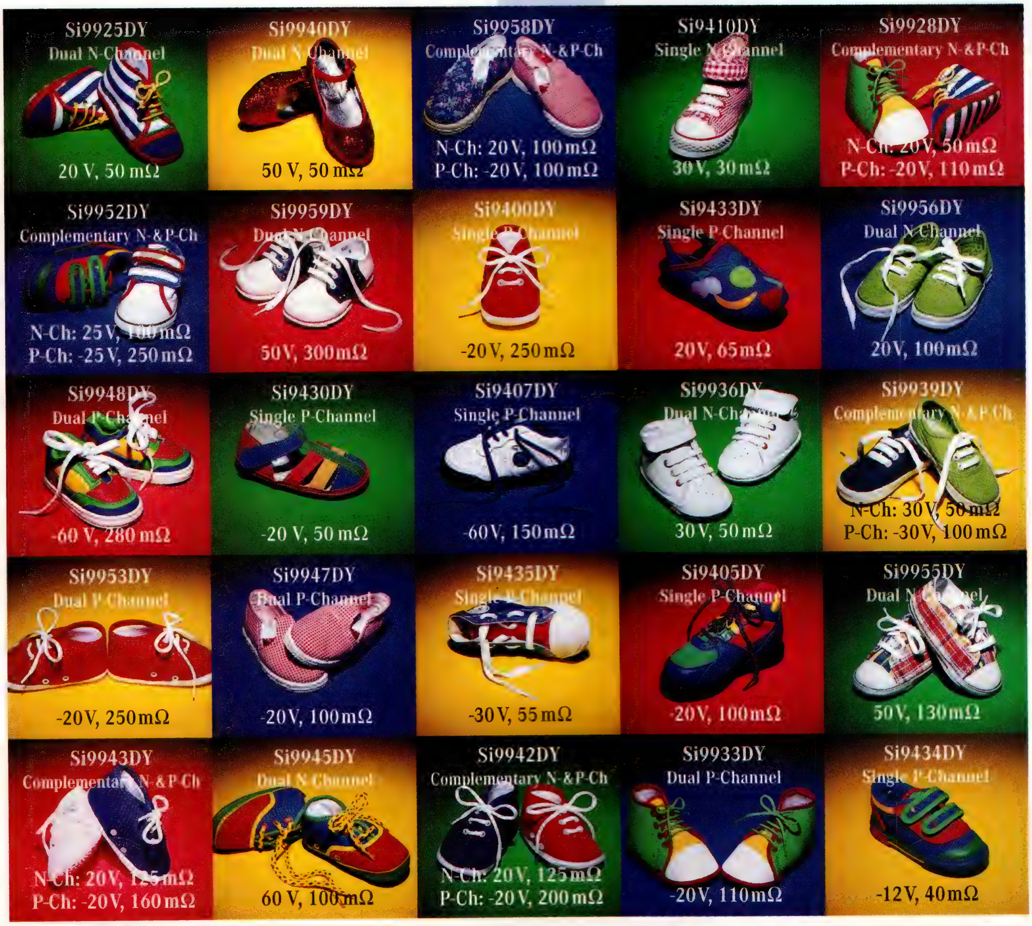

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IEEE Conference on Computer Vision & Pattern Recognition, June 20-24. The Westin Hotel, Seattle, WA. Contact IEEE Computer Society, Conference Dept., 1730 Massachusetts Ave. NW, Washington D.C. 20036-1992; (202) 371-1013; fax (202) 728-0884.

IEEE Antennas & Propagation Society International Symposium & URSI National Radio Science Meeting, June 20-24. University of Washington, Seattle, WA. Contact Akira Ishimaru, University of Washington, Dept. of Electrical Engineering, FT-10, Seattle, WA 98195; (206) 543-2169.

International Conference on Applications of Photonic Technology Sensing, Signal Processing & Communications (ICAPT), June 21-23. Hilton International Hotel, Toronto, Ontario, Canada. Contact George A. Lampropoulos, A.U.G. Signals Ltd., 560 Lauder Ave., Toronto, Ontario, M6E 3J6, Canada; (905) 658-6353; fax (905) 654-6310; E-mail: lampro@utcc.gpu.utoronto.ca.

European Fibre-Optic Communications & Networks (EFOC&N '94), June 22-24. Heidelberg, Germany. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA; (617) 232-3111; fax (617) 734-8562.

IEEE 3rd International Fuzzy Systems Conference, June 26-29. Walt Disney World Dolphin Hotel, Lake Buena Vista, FL. Contact Steve Marlin, Meeting Management Inc., 2603 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444.

9th Conference on Computer Assurance (Compass '94), June 27-July 1. National Institute of Standards and Technology, Gaithersburg, MD. Contact John McLean, (202) 767-3852; fax (202) 404-7942.

Conference on Precision Electromagnetic Measurements (CPEM '94), June 27-July 1. Clarion Harvest House Hotel, Boulder, CO. Contact Donald B. Sullivan, Div. 847, National Institute of Standards and Technology, Boulder, CO 80303-3328; (303) 497-3772.

IEEE International Conference on Neural Networks (ICNN '94), June 28-July 2. Walt Disney World Dolphin Hotel, Lake Buena Vista, FL. Contact Steve Marlin, Meeting Management Inc., 2603 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444.

American Control Conference, (ACC '94), June 29-July 1. Stouffer Harbor Place Hotel, Baltimore, MD. Contact Hassan Khalil, Dept. of Electrical Engineering, Michigan State University, East Lansing, MI 48824; (517) 355-6689; fax (517) 353-1980.

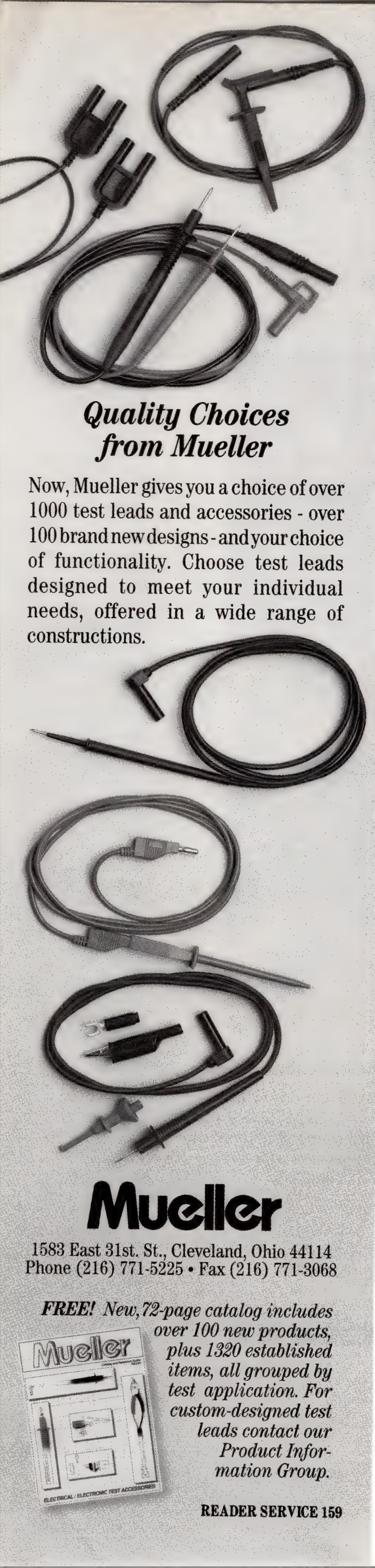
JULY

1st IEEE International Workshop on Community Networking, July 13-14. Westin Hotel, San Francisco, CA. Contact Riccardo Guisella, Hewlett-Packard Labs., 1501 Page Mill Rd., MS 1 U-17, Palo Alto, CA 94304; (415) 857-7687; fax (415) 857-8526.

1994 IEEE Nuclear & Space Radiation Effects Conference (NSREC), July 18-22. Westin La Paloma Resort, Tucson, AZ. Contact Charles J. Utrias, NSREC vice chairman for publicity, United Technologies, Microelectronics Center, 1575 Garden of the Gods Rd., Colorado Springs, CO 80907; (719) 594-8035; fax (719) 594-8187.

2nd IEEE Workshop on Real-Time Applications, July 21-22. Washington D.C. Contact Alexander D. Stoyenko, Real-Time Computing Lab, Computer & Information Science, New Jersey Institute of Technology, University Heights, Newark, NJ 07102; (201) 596-5765; fax (201) 596-5777; E-mail: Alex@vulcan.njit.edu.

IEEE Power Engineering Society Summer Meeting, July 24-28. Hilton Hotel, San Francisco, CA. Contact Eva Tiffer, Pacific Gas & Electric Co., Mail Code B23C, P.O. Box 770000, San Francisco, CA 94105; (415) 973-2875; fax (415) 972-6011.



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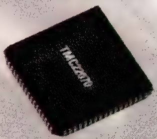

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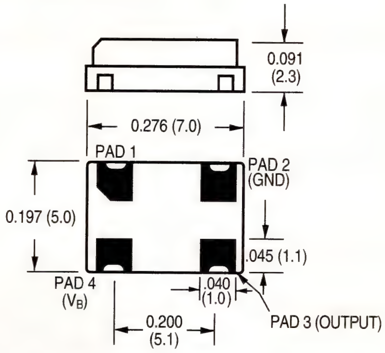

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UPCOMING MEETINGS

AUGUST

3rd IEEE International Symposium on High Performance Distributed Computing, Aug. 3-5. Westin St. Francis Hotel, San Francisco, CA. Contact Geoffrey C. Fox, NPAC Director, Room 3-228, 111 College Pl., Syracuse, NY 13244-4100; (315) 443-4741; fax (315) 443-1973; E-mail: Gcf@pac.syr.edu.

4th IEEE Workshop on Computers in Power Electronics, Aug. 7-10. The Universite du Quebec, Trois-Rivieres, Quebec, Canada. Contact Adam Skorek, Dept. d'Ingenierie, UQTR, C.P. 500, Trois-Rivieres, Quebec G9A 5H7, Canada; (818) 376-5071 ext. 3929; fax (819) 376-5152.

IEEE International Symposium on Applications of Ferroelectrics, Aug. 7-10. Conference Center, University Park, PA. Contact Amar Bhalla, 253 MRL, Pennsylvania State University, University Park, PA 16802; (814) 865-9232.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '94), Aug. 8-12. California Institute of Technology, Pasadena, CA. Contact Tammy I. Stein, IEEE/GRSS, 2610 Lakeway Dr., Seabrock, TX 77586; (713) 291-9222; fax (713) 291-9224.

IEEE Magnetic Recording Conference (IMRC '94), Aug. 16-20. University of California, La Jolla, CA. Contact Roger F. Hoyt, IBM Almaden Research Center, 650 Harry Rd., K01/803, San Jose, CA 95120-6099; (408) 927-2118; fax (408) 927-3204.

IEEE International Symposium on Electromagnetic Compatibility, Aug. 22-26. Palmer House Hotel, Chicago, IL. Contact H.R. Hofmann, 1210 Lawn Meadow Ln., Naperville, IL 60540; (708) 979-3627; fax (708) 979-5755.

Conference on Lasers & Electro-Optics, Europe & The 5th European Quantum Electronics Convention (CLEO EUROPE/EQEC), Aug. 28-Sept. 2. RAI Congress Centre, Amsterdam, The Netherlands. Contact Susan Evans, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3896; fax (908) 562-1571.

SEPTEMBER

IEEE International Symposium on Compound Semiconductors, Sept. 18-22. Del Coronado Hotel, San Diego, CA. Contact James Harbison, Bellcore, 331 Newman Springs Rd., Room 3X-211, Red Bank, NJ 07701; (908) 758-3386; fax (908) 758-4372.

14th IEEE International Semiconductor Laser Conference, Sept. 19-23. Hyatt Regency Maui, Maui, HI. Contact Samantha H. Phillips, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331; (908) 562-3894; fax (908) 562-1571; E-mail: s.phillips@ieee.org.

ASIC Conference and Exhibit (ASIC '94), Sept. 19-23. Rochester Riverside Convention Center, Rochester, NY. Contact Paul P.K. Lee, Eastman-Kodak Co., Rochester, NY 14650-2008; (716) 477-2869; fax (716) 477-4947.

AUTOTESTCON '94, Sept. 20-22. Disneyland Hotel, Anaheim, CA. Contact Robert Rassa, ManTech International, 150 S. Los Robles Ave., Suite 350, Pasadena, CA 91101; (818) 577-7100; fax (818) 577-7102.

Canadian Conference on Electrical and Computer Engineering, Sept. 25-28. World Trade & Convention Centre, Halifax, Nova Scotia, Canada. Contact C. Robert Baird, Dept. of Electrical Engineering, Technical University of Nova Scotia, P.O. Box 1000, Halifax, Nova Scotia, B3J 2X4 Canada; (902) 420-7717; fax (902) 422-7535.

Information Superhighway Summit/San Jose, A ComNet Conference, Sept. 26-28. Red Lion Hotel, San Jose, CA. Contact Jeff Silha, IDG World Expo, (800) 225-4698 or (508) 820-8628.

WESCON '94, Sept. 27-29. Anaheim Convention Center, Anaheim, CA. Contact Joan Carlisle, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (310) 215-3976; fax (310) 641-5117.

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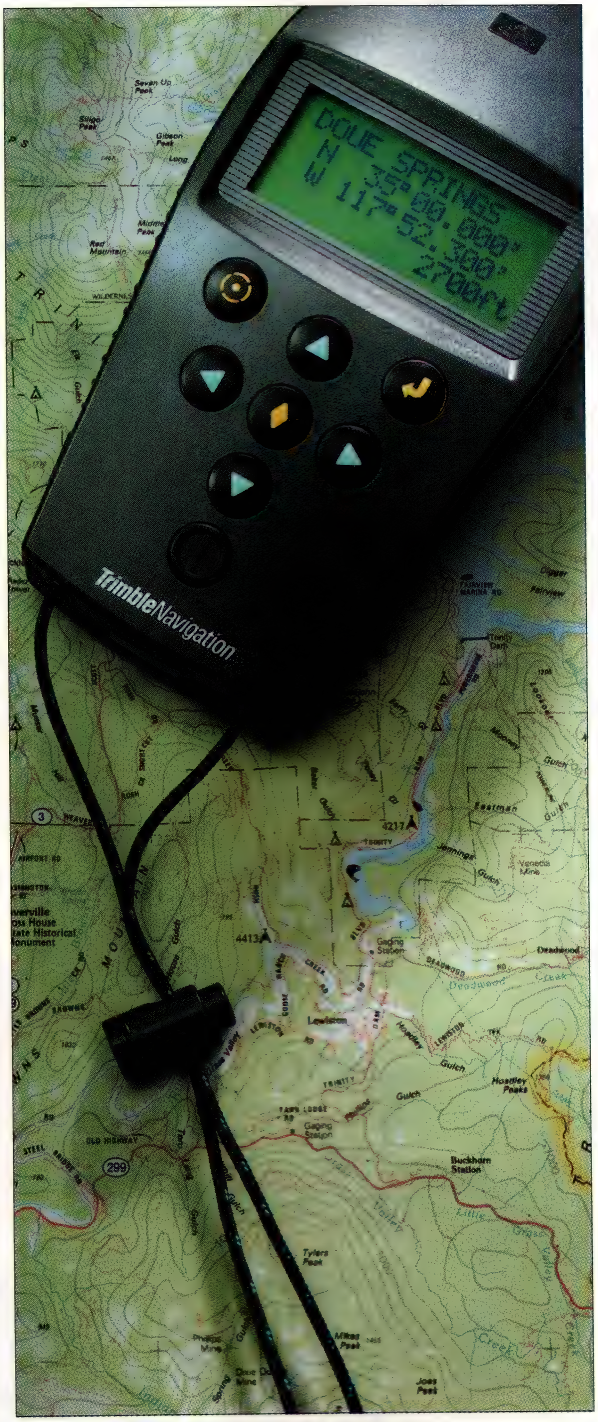

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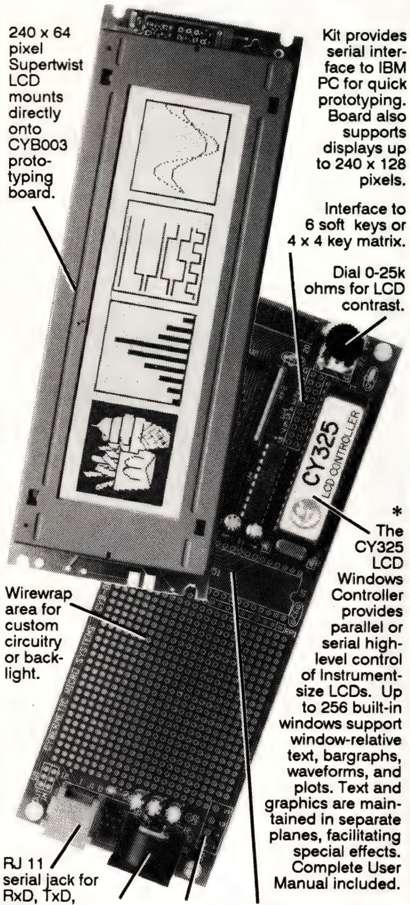

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OVER THE WALL

The magazine business works this way: The editor writing an article composes a stream-of-consciousness mixture of sentence fragments and throws it "over the wall" to the editor managing the article. He or she reconstructs it as best they can and throws it back for review. The cycle is repeated on down the line toward publication. It's somewhat reminiscent of a large snake digesting an egg with many hiccups along the way.

Obvious analogies can be drawn in engineering. Unfortunately, what results are longer cycle times and products that could be better. The solution is concurrent engineering, and it's being implemented everywhere. But old habits die hard. The over-the-wall modus operandi is deeply ingrained.

Case in point: The Portable By Design Conference. We set up the technical sessions to cover the entire design process from components to ergonomics. Our technical advisory committee concurred with the plan. At the committee's request, we added sessions on mechanical engineering and recruited top-notch people. One was Dennis Boyle of Ideo Product Development, who designed Apple's Duo-Dock systems. Another was Gary Kuzmin of Aavid Engineering, the company that designed a cooling system for Pentium-type portables.

Gary's paper didn't focus narrowly on how to cool portable equipment. Rather, he discussed how EEs and MEs can work together to design products that don't require exotic cooling systems. His paper confronted the "over-the-wall" theory of system design.

Attendance at the mechanical sessions was mediocre, but the interaction among the 30 to 40 engineers (mostly enlightened EEs, I might add) was intense. Judged in that light, I think those who attended went away with a competitive edge.

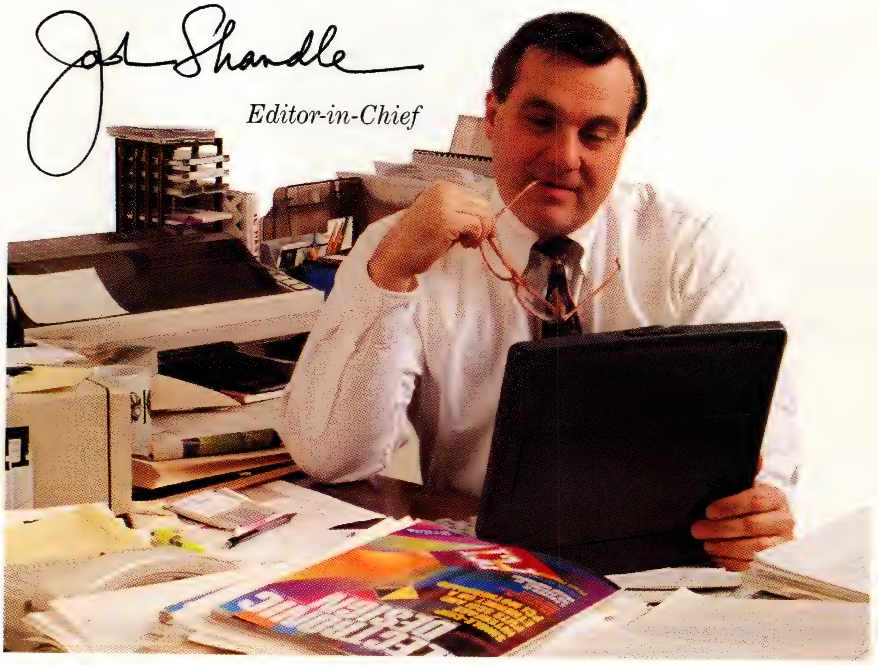
On the other hand, the sessions on the "core interests" of our EE readers were well attended. With luminaries like Linear Technology's Jim Williams delivering papers, this is to be expected. In my view, attending these sessions kept people up to speed but did not offer a real competitive edge.

I'm not suggesting that engineers avoid sessions which address their specific job. But I do believe that with portable systems, in particular, the over-the-wall psychology will inevitably lead to an over-the-hill product.

In many ways, portable designs constitute a brand new ballgame. Every member of the design team should share responsibility for the total design.

Josh Shandle

Editor-in-Chief



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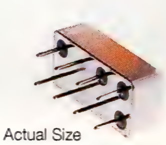

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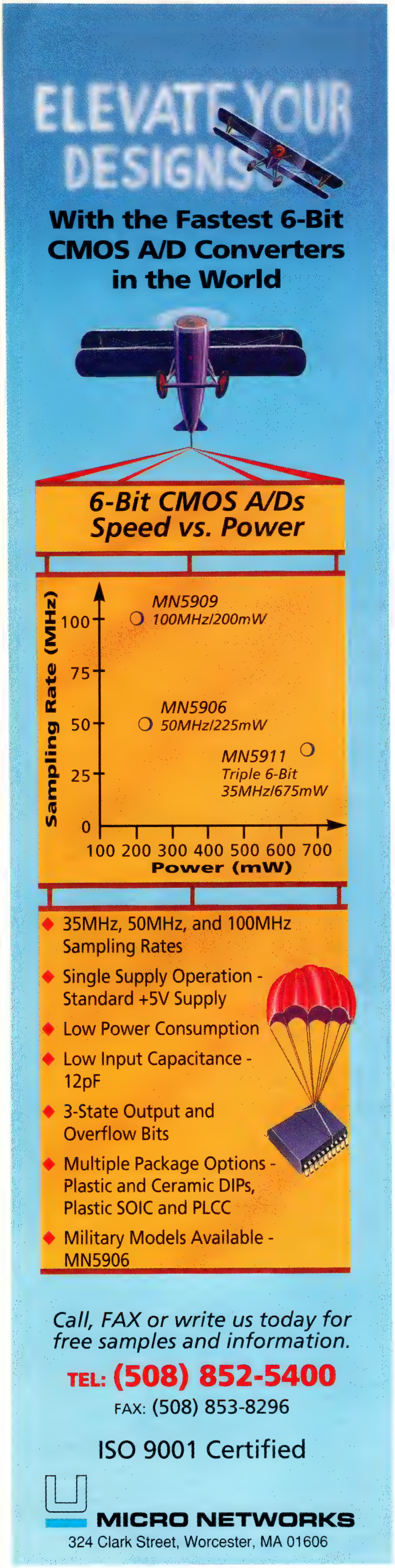

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TECHNOLOGY BRIEFING

OBSERVATIONS OF A TIME TRAVELER

Time travel is very educational. I recommend it highly. If you can't afford a time machine, the next best thing is the aerospace industry. After laboring ten years in the isolated, technically conservative aerospace culture, I emerged from my time capsule and came to work at Electronic Design. Not surprisingly, electronics had changed a bit since 1984.

Many of these changes are impressive, but predictable. It would have been a no-brainer to predict the trend toward smaller, faster, cheaper, and more complex. However, there are a few developments that I'm still having trouble comprehending. ICs with 600 pins take some getting used to and 128-processor systolic-array DSPs-on-a-chip give me a distinct feeling of future shock.

Stranger yet, many of the most significant advances weren't technical in nature. Take, for instance, the phenomenon of strategic alliances. Even the largest companies are sharing resources and expertise to produce increasingly complex products in a timely, cost-effective way.

This isn't some passing fad like "right-sizing" or Taguchi theory, this is the future of electronics. In my view, one of the prime reasons that many Asian industries have become so successful lies in their ability to form alliances much more quickly than their ruggedly individualistic American counterparts.

What are these mysterious alliances anyway? The general consensus is that a strategic alliance is more than a simple agreement to mutually buy and sell products, but less than a corporate merger.

Within this gray area is an exciting spectrum of relationships that include technology exchanges,and cooperative development projects. Steve Sharp of TriQuint Semiconductor put it nicely when he described strategic alliances as "two or more companies sharing a co-destiny in a specific area."

LEE GOLDBERG
COMMUNICATIONS

Perhaps the most unexpected partnering I've stumbled upon so far is the Apple/IBM/Motorola alliance. Who could anticipate that IBM would join with it's arch-rival Apple to develop a common operating system, and then spurn Intel to develop a new CPU with Apple's favored chip-maker, Motorola?

But you needn't be a giant to benefit from a strategic alliance. Consider, for example, Chip Express. This small, fabless company provides rapid prototypes of custom ASIC chips. They can turn a standard net list into a packaged, ready-to-run chip in just 24 hours using laser-programmable interconnects.

What makes this possible is Chip Express' special relationship with Yamaha Semiconductor. The company licensed its programmable metal technology to Yamaha, which provides the silicon for the prototype service. Yamaha, in turn, benefits first by selling silicon to Chip Express. But most important for both companies is that the same tapes that were used for the prototype can be used to make production ASICs by programming standard chips with a metal layer.

AT&T and TriQuint Semiconductor have also developed a synergistic relationship. As AT&T developed more wireless and fiber-optic products, GaAs became a critical strategic technology. TriQuint is a medium-size firm with modern, cost-effective GaAs production facilities producing high-quality GaAs products which easily interface to their companion silicon components.

Rather than attempt to duplicate this technology, AT&T chose to shut down its own GaAs fab line and transfer its proprietary designs to TriQuint. In this arrangement, TriQuint gained a large steady customer while AT&T secured priority access to high-performance technology at a fraction of the cost of developing it alone. While both companies still retain autonomy, they have become interdependent, which is a hallmark of these new alliances.

If things have changed this much in ten years, I wonder what the next decade will bring. I guess I'll just have to hook up the flux capacitor in the old DeLorean and go find out.

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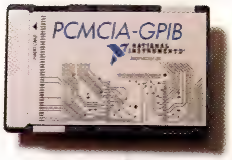

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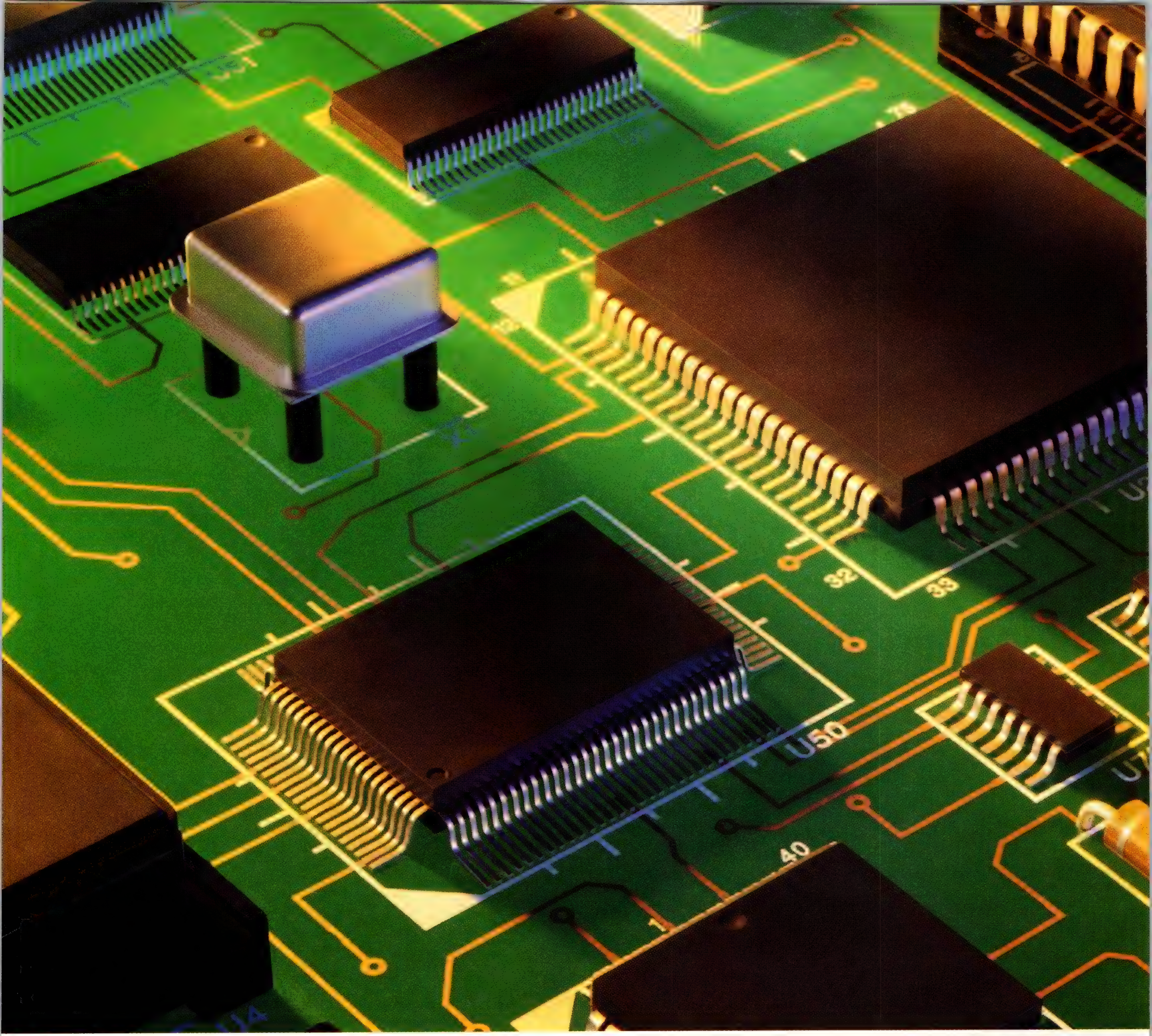

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iFX760	60	10ns	60	1.5mA/MHz
iFX740	40	10ns	50	1mA/MHz
iFX730	30	10ns	30	1mA/MHz

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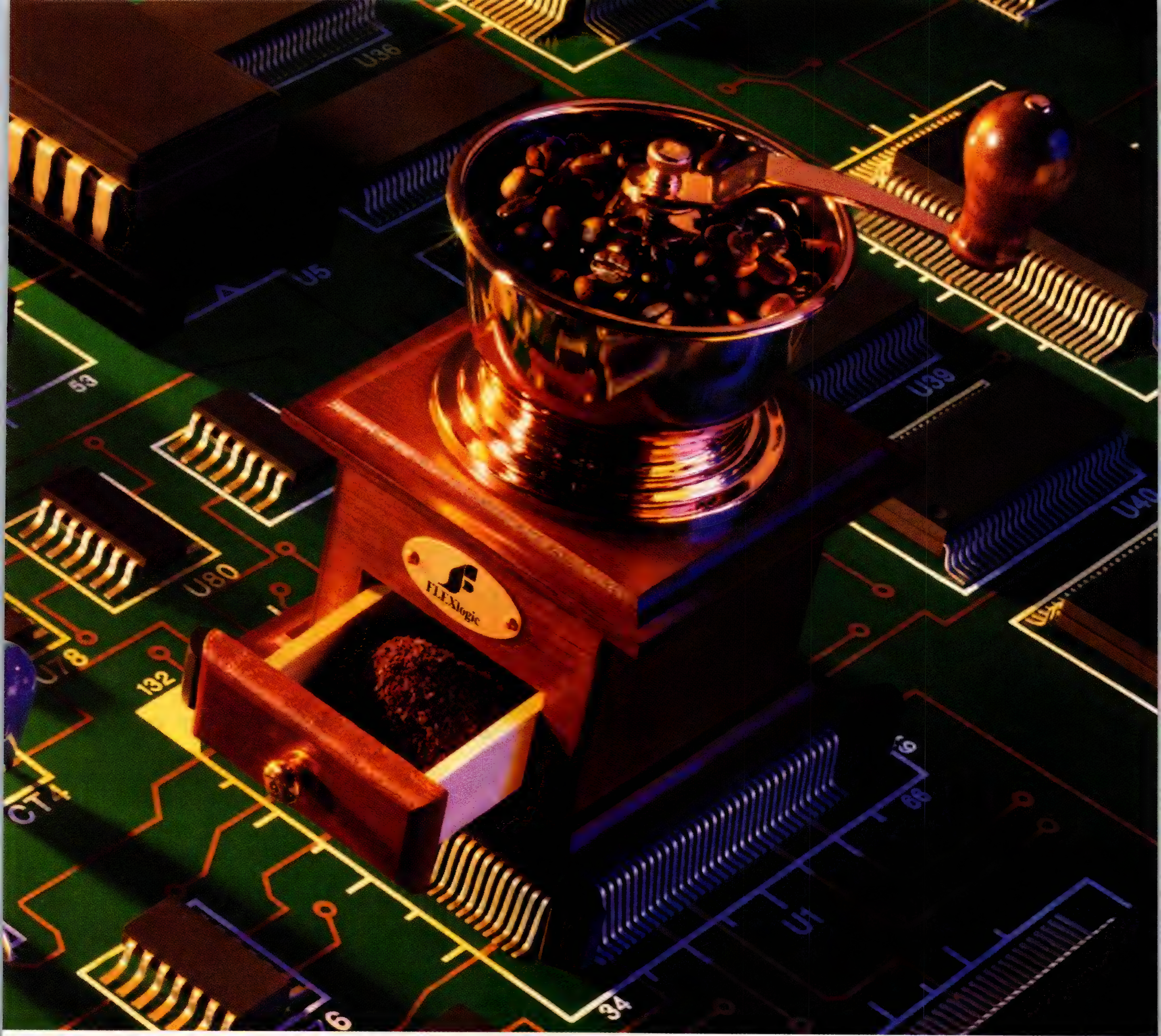

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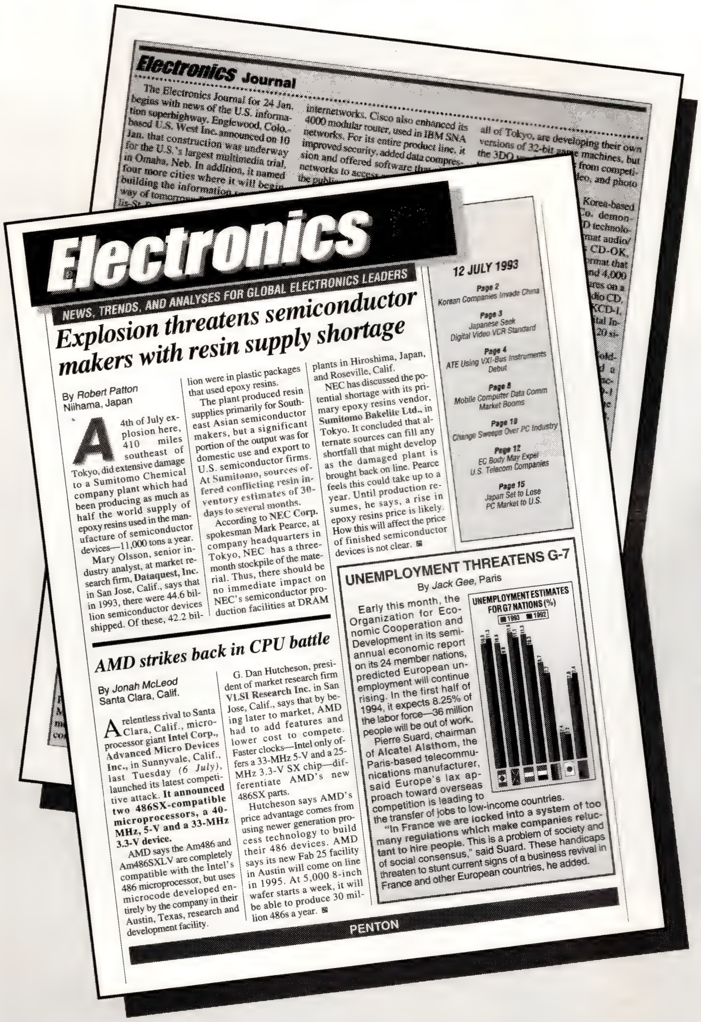

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial in Omaha, Neb. In addition, it named four more cities where it will begin building the information

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ■

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AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ■

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of Alcatel Alsthom, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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TECHNOLOGY NEWSLETTER

MESHING SCHEME YIELDS ACCURATE SIMULATIONS

By using selective and controllable computational-meshing techniques, a new thermal-management tool can perform model simulations as accurately as possible with minimal computation cost. The IcePak thermal-management software developed by Fluid Dynamics International, Evanston, Ill., automatically creates an optimal mesh, generating refinements according to design principles that dictate where emphasis should be placed. IcePak analyzes air flow and thermal distribution in enclosed spaces, particularly those containing electronic components. The tool's unique cocooning approach governs mesh generation near and around all objects in a model, increasing the element density by refining the mesh automatically around objects. The package also evaluates mesh quality, identifying poor quality elements for correction. Users then can specify a tighter mesh for the distorted elements, or refine contiguous elements around an object to improve the mesh quality. For more information on IcePak, call (708) 491-0200. *LM*

INTERFACE-SIMULATION MODEL ACCURACY EYED

Present molecular models of water, which are used in computer simulations and statistical calculations to predict properties of electrode/electrolyte interfaces, may now have to be redrawn for accuracy. That's because researchers at the IBM Almaden Research Center, San Jose, Calif., discovered that increasing the voltage of a metal electrode causes water molecules to crowd together to produce a packing factor of up to double the water's liquid density. The discovery came during an X-ray scattering study. As part of the study, silver crystal was contained in a specially designed cell and immersed in water. X-ray beams were aimed at the crystal's surface and their scattering patterns were analyzed to determine the orientations of the water molecules. Not only did water molecules organize into discrete layers near such metal surfaces, but the predicted rotation of the water molecules' orientation (from oxygen-up to oxygen-down) was changed from negative to positive when a voltage was applied. The most interesting result, though, was that as the voltage on the electrode was raised, the liquid density doubled. These results dramatically alter how surface reactions occur on an atomistic level. Contact Michael Ross of IBM at (408) 927-1283. *CA*

SENSORS USED FOR FLAW DETECTION

By measuring the perturbations in spatially resolved electric fields, high-resolution measurements of surface and internal subsurface features, on either conductive or non-conductive workpieces, respectively, may be made with capacitance and impedance sensors. Developed at Sandia National Laboratory, Albuquerque, N.M., the sensors are the result of ongoing research and development within the microelectronics division. One sensor that was recently developed and evaluated, the high-resolution capacitance imaging sensor (HIRCIS), can generate surface images and track features. For example, when applied to surface imaging of burrs on metal workpieces, the HIRCIS enables closed-loop feedback control of automated deburring systems. An extra advantage of this sensor is that it can accurately detect metal burrs of less than 10 μm in height and chamfers ranging from 50 to 350 μm. Its ability to achieve a resolution of 25 μm in less than a second, as well as other capabilities, suit it for in-process control of precision operations. Future applications of this sensor are expected to boost manufacturing reliability and throughput. For more information, contact Jim Novak of Sandia National Laboratory at (505) 844-4227. *CA*

MULTIPROCESSOR SPEC DEFINES MP PLATFORMS

Multiprocessor-platform (MP) operating systems now can run on specification-compliant systems thanks to an MP specification that puts in place a standard hardware/software interface. Systems based on the specification will be able to run next-generation MP operating systems while maintaining compatibility with all existing application software. The multiprocessor specification version 1.1 was developed by the Intel Corp. Architecture Laboratories, Santa Clara, Calif., in conjunction with system manufacturers, BIOS suppliers, and operating-system vendors. MP-specification-compliant operating systems will include Microsoft Windows NT, Novell's NetWare and UnixWare, IBM's OS/2 for SMP, The Santa Cruz Operation's MPX, and SunSoft's Solaris. System manufacturers have begun designing MP workstations and servers based on Intel's Pentium processor, and many BIOS suppliers also are developing compliant products. Most products are expected to be introduced in the last quarter of this year. To obtain a copy of the MP specifica-

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tion, contact any Intel sales office or call (800) 548-4725 (U.S.); (916) 356-2746 (outside the U.S.). *DB*

IMAGER PRODUCES SMALL, INEXPENSIVE DISPLAYS

A smart slide imaging device, based on single-crystal silicon technology, makes it possible to fabricate lightweight, portable, high-density, and high-picture-quality active-matrix liquid-crystal displays (AMLCDs) and head-mounted-display (HMD) products. Developed and implemented by Kopin Corp., Boston, Mass., in cooperation with MIT Lincoln Laboratory, Cambridge, Mass., the device is the result of a Cooperative Research and Development Agreement signed in Oct. 1993. The smart slide with its integrated circuitry is fabricated on thin-film, single-crystal silicon, using standard IC processing, and then transferred onto glass. This process allows for a substantial improvement in display quality and manufacturability. The device has a resolution of 1100 lines/in.^{2} in a 0.5-by-0.5-in. chip. It also contains 300,000 transistors in an active area of 0.25 in.^{2} and control electronics, all monolithically integrated with the display. Its fast frame rate of 60 Hz allows for full video-speed connection to all types of personal computers. For further information, contact Paul Mitchell of Kopin at (508) 824-6696. *CA*

NATIVE CODE SPEEDS VERILOG SIMULATIONS

Native-code simulation technology increases speed by skipping over the compilation phase to directly generate executable code. Using that technology, the newest version of the Verilog Compiled Simulator (VCS) from Chronologic Simulation, Los Altos, Calif., reduces the time needed to process a model for simulation by at least a factor of four. Up to now, VCS has generated C code that was compiled by commercial compilers to produce object files for simulation. The VCS native-code generator reduces the time needed to create object files. In addition, it also streamlines the code by using optimization techniques specifically designed for the Verilog hardware description language—something that standard C compilers aren't designed to do. Direct-code generation reduces the overall time it takes to modify a model, which is appealing for the iterative design and debug phase of system design. The native-code-generation version of VCS runs on HP and Sun workstations. Call (415) 965-3312 for more information. *LM*

MCM SERVICE SPEEDS DESIGN TURNAROUNDS

Reducing risk in multichip-module (MCM) implementations is a big concern for designers, and a consulting-services program intended to improve MCM adopters' processes, shorten design cycles, and smooth the way to advanced packaging techniques helps move toward that goal. The MCM Pilot and Manufacturing Process Optimization program developed by Harris EDA Inc., Fishers, N.Y., delivers a working prototype of an MCM design and transfers MCM design experience to the host development team. Clients of the program gain access to the tools and expertise they need to minimize the risk of applying MCM technology to their current- and next-generation designs. Through the Harris program, would-be MCM implementers learn to evaluate the technology's feasibility for their products, design and partition circuits to maximize the benefits of using MCMs, evaluate the various MCM options, and find and work effectively with MCM foundries. For more information, contact Harris EDA at (716) 924-9303. *DM*

CVD REACTOR TO ADVANCE IC PROCESSING

Attempts to develop a new chemical-vapor-deposition (CVD) reactor for the production of high-quality intermetal dielectrics is the prime focus of a $6 million cooperative research and development agreement (CRADA) between Sandia National Laboratory, Albuquerque, N.M., and Lam Research Inc., Fremont, Calif. Using hydride-based reactants for film deposition, the companies will examine new techniques for depositing a high-quality planarizing intermetal dielectric at low temperature. Their combined efforts will be geared toward solving the problems typically associated with the insulating layer between metal levels: poor conformity, lack of planarization, high stress, water retention, and cracking. Results of this CRADA are expected to yield high-quality intermetal dielectrics, which may be used for the production and future advancement of ICs. For more information, contact Sandia National Laboratory at (505) 844-7767. *CA*

X-RAY IMAGER ENABLES FUTURE MICROCIRCUITS

Sandia National Laboratory also has teamed up with GCA Tropel, Fairport, N.Y., to develop an ultra-precise, vacuum-compatible housing for a soft X-ray projection lithography (SXPL) imaging system. The results of this joint study, as part of $2.35 million CRADA, are expected to lead to the eventual fabrication of a new generation of microcircuits. Recent tests already show that features of microelectronic circuits as small as 0.05 μm can be printed using a laser plasma source. Future efforts by the

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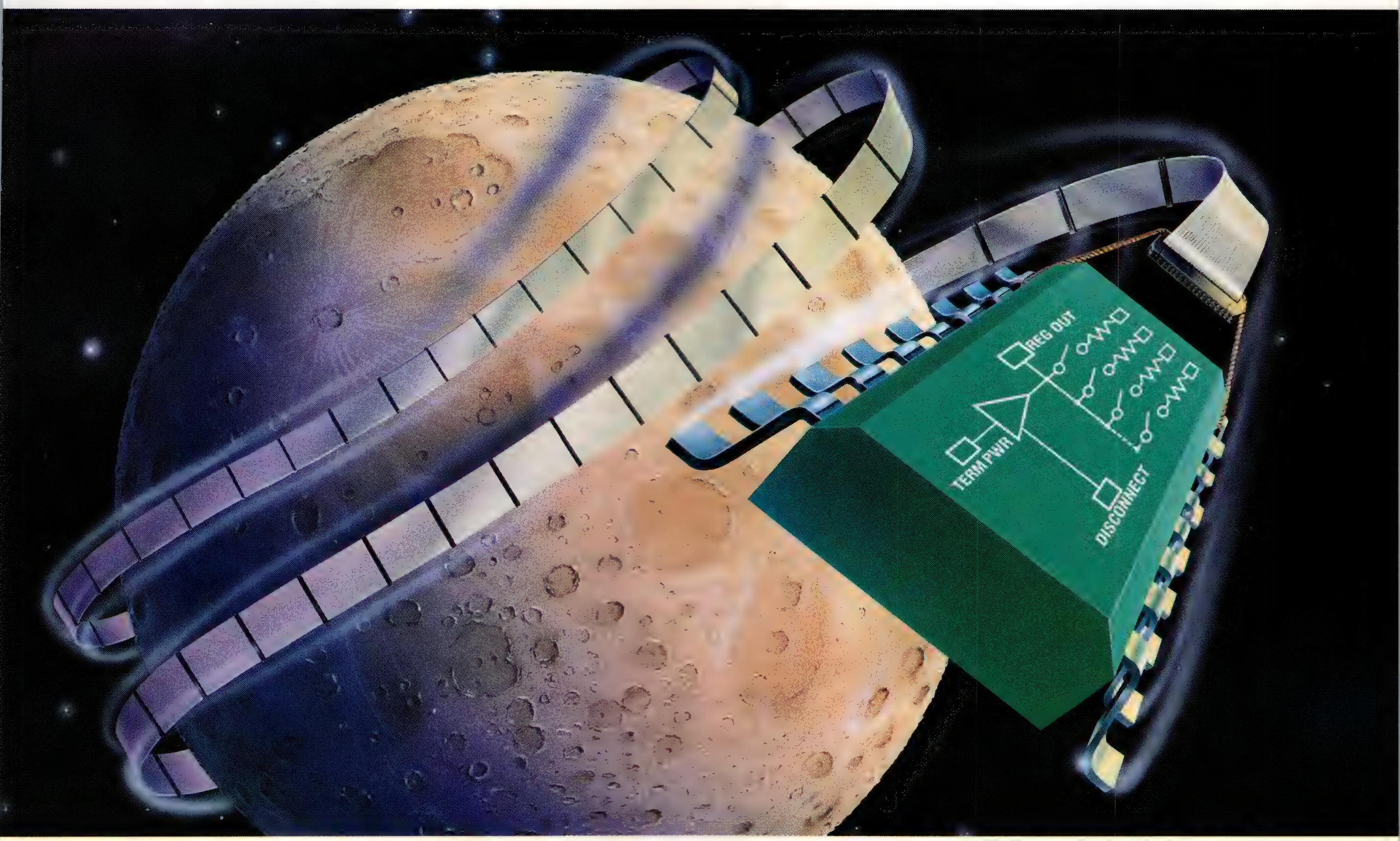

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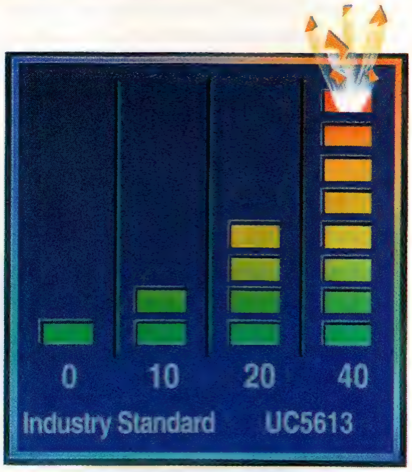

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New TV signal encoders

For use in consumer and semi-professional video equipment, the TDA8501 and TDA8505 signal encoders convert RGB or YUV video inputs into composite video signals to PAL/NTSC or SECAM standards. They combine maximum flexibility with minimum external component needs and circuit alignment operations.

Reader Service 225

LCD controller generates all display drive voltages

The PCF2116X display controller provides a unique single-chip, single-supply-rail solution for driving 2x24 or 4x12 dot matrix LCDs. It features on-chip generation of the LCD's negative supply voltage plus all its intermediate bias voltages and requires just two external components.

Reader Service 226

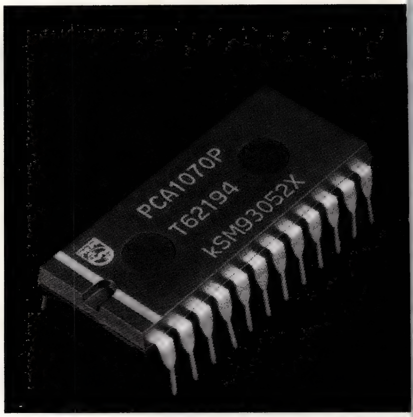
Line interface IC adapts to telephone systems worldwide

The new PCA1070 multistandard speech transmission/line interface IC has the unique ability to adapt to virtually all standard telephone line conditions encountered around the world, enabling manufacturers to produce a single telephone set design for sale in international markets. In addition to the cost savings associated with higher volume set manufacture, the PCA1070's need for very few external components further reduces production costs.

Controlled via the I²C-bus by a low-voltage low-power CMOS microcontroller, programmable characteristics of the PCA1070 include DC and AC set impedance, sidetone balance, earpiece and microphone amplifier gain, line signal dynamic limiting and hearing protection levels.

Programming the IC to suit different telephone line conditions is performed entirely under software control and does not involve any changing of external components. The PCA1070 also has the ability to measure the available line current and to pass this information to the microcontroller over the I²C-bus, allowing interface parameters to be further modified so that the telephone continuously adapts to changing line conditions.

The PCA1070 is suitable for use in a wide range of telephone equipment including conventional telephone sets, cordless phone base stations (analog CT0, CT1 as well as digital CT2, DECT and PHP), fax machines, answering machines and payphones.



The PCA1070 multistandard speech transmission/line interface IC can adapt to virtually all standard line conditions met worldwide.

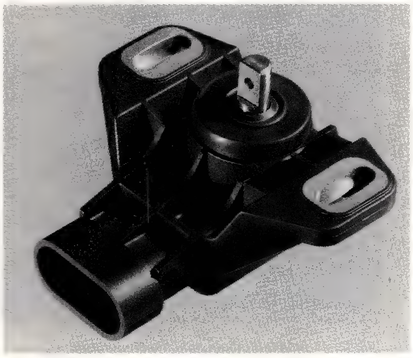
Reader Service 224

Contactless angular-displacement sensor is encapsulated and ready-to-use

The new KMA10/70 contactless sensor provides a fully-encapsulated, non-wearing and adjustment-free solution to angular position measurement in a wide range of automotive and industrial applications such as active suspension units, accelerator pedal position sensing and servo control actuators. Its sealed housing, wide operating temperature range and high degree of EMC protection make it particularly useful in safety-critical applications.

Based around the Philips KMZ11B1 magneto-resistive sensor element, the KMA10/70 has an integral input shaft which rotates the magnetic field over the sensor element. The resultant changes in the sensor element's resistance are detected by a thick-film hybrid signal conditioning circuit which produces a temperature-compensated 4 to 20 mA output signal that corresponds to the angular displacement of the input shaft. The sensor has a displacement range of ±35° and is free from the microlinearity error and noise problems associated with potentiometers, particularly when these devices suffer wear and corrosion.

The KMA10/70 has an operating temperature range of –40 to +100°C and a lifetime in excess of 10^8 operating cycles. It is a 3-terminal device which operates over an 8.1 to 11.0 V supply voltage range, producing a short-circuit-protected, current-mode output which is independent of supply voltage changes.



The KMA10/70 contactless angular-displacement sensor is fully-encapsulated to survive extreme environmental conditions.

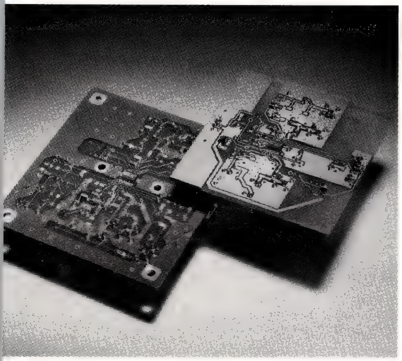
Reader Service 227

Philips Semiconductors

ow-voltage low-power requency synthesizers for mobile ommunication systems

ree new dual-frequency synthesizer ICs offer the vest power dissipations per synthesizer currently ailable, coupled with unimpaired operation at pply voltages as low as 2.7 V. Between them, ese devices cover the frequency range 400 MHz 2.4 GHz, with each device being optimized r use in particular mobile phone systems. e UMA1015M serves CT1/CT1+ cordless and MPS/(E)TACS/NMT analog cellular systems, the MA1018M serves GSM and the UMA1020M CS1800 and DECT systems. The UMA1020M the only dual synthesizer in the world to offer 4 GHz synthesis from a 2.7 V supply. All three nthesizers are also suitable for a wide range of her RF frequency synthesis applications.

All the synthesizers feature two independent equency synthesis loops, direct drive to a voltage-ntrolled oscillator, and an auxiliary output port DAC to control other handset functions. With rrent consumption of typically only 10 mA, wer-down modes which reduce standby power nsumption to just 20 µA, plus high-speed on/off itching capabilities, these ICs can dramatically crease time between battery charges in hand-rtable telephones.



ew dual-frequency synthesizer ICs mean that Philips now ovides low-voltage low-power solutions to RF frequency nthesis in handsets for all the latest mobile phone systems.

The synthesizers are controlled via a high-speed ree-wire serial interface which, in addition to ntrolling the programmable dividers, charge-pump perating modes and auxiliary control outputs or AC, also controls the ICs' power-down modes. he devices are fabricated in Philips' QUBiC iCMOS process to achieve the necessary mbination of high speed and low power nsumption.

Reader Service 228

New single-chip microcontroller and CAN controller

Designed for automotive and industrial multiplex wiring applications, Philips Semiconductors' new IC combines the functionality of the high-performance P83C552 8-bit microcontroller with the PCA82C200 stand-alone CAN controller. The new IC, the P83C592, has all the features required for embedded control – high-speed prioritized interrupts, on-chip event counters and timers, multi-channel A/D conversion, PWM outputs and digital I/O ports – plus an on-chip CAN (Controller Area Network) interface that allows it to communicate with other intelligent CAN modules in distributed real-time control systems.

The P83C592's CAN interface is a full implementation of the CAN specification and provides all the physical and data link layer functions of the OSI communications model. It can recognize all 2032 types of CAN message identifier and so can be used in systems where both low-speed and high-speed prioritized data communications are required on the same network. This is particularly important in automotive applications, which require high-speed real-time communication (up to 1 Mbit/s) between critical systems such as ABS and engine-management systems, as well as low-speed communications for on/off control of lights, motors, solenoids, etc.

The P83C592 microcontroller incorporates a CAN interface which suits it for automotive and industrial multiplex wiring applications.

The new device provides 16 kbytes of on-chip ROM and a 256-byte dual-port RAM which operates as a transmit/receive buffer for CAN messages. The microcontroller is also available in EPROM and ROM-less versions, designated P87C592 and P80C592 respectively, with all versions having a maximum RAM and ROM addressing range of 64 kbytes. The P83C592 is available with a –40 to +125°C operating temperature range specifically for automotive applications; standard operating temperature range for the three devices is –40 to +85°C.

Reader Service 229

Evaluation kit permits field testing of smartcards

Using the new OM4281 evaluation kit, software developers writing code for the Philips P83C852 smartcard microcontroller can now verify operation of their completed application program independently of any development system.

The kit, which is intended to be used during the last phases of software development, after normal emulation and program debugging have been completed, provides users with an intermediate step between leaving the development system environment and having to embed a mask-programmed microcontroller into smartcard plastic.

The kit comprises a smartcard simulation pc board with ISO-standard card reader contacts on it, which connects via a ribbon cable to a second small pc board that carries a 68-lead bond-out version of the P83C852 and a 28-pin EPROM socket for application firmware. These two pc boards form a self-contained unit which can be used to field-test the smartcard application. When the user is happy that the application works, the bond-out P83C852 and EPROM can be replaced with a mask-programmed version of the micro-controller. This plugs into a socket which is mounted directly on the smartcard simulator pc board, allowing this board then to be used without the second pc board and ribbon cable.

The P83C852 is an 80C51-based smartcard microcontroller with a unique on-chip arithmetic unit that dramatically increases the speed with which public-key crypto algorithms can be computed. In addition to this arithmetic unit, it includes 6 kbytes of ROM, 256 bytes of RAM and 2 kbytes of EPROM.

Reader Service 230

13/6/94 US ED

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READER SERVICE 95

two organizations will be to further develop the imaging system, as well as locate or identify a suitable stable housing for the system that can operate in a vacuum. For more details, contact Sandia National Laboratory at (505) 844-7767. *CA*

FED PROTOTYPE ADVANCES DISPLAY TECHNOLOGY

An early field-emission display (FED) prototype featuring a monochrome video rate display with 700-pixel/in. resolution and associated solid-state electronics, is anticipated to exceed the image quality of active-matrix liquid-crystal displays (AMLCDs) and at a much lower cost. According to the scientists at Micron Display Technologies Inc., Boise, Idaho, who developed the FED prototype, this is only the beginning. Future portable-display products, and other products such as full-immersion HMDs, show strong potential for the use of FED flat-panel technology. Currently under a contract from ARPA, the company will further pursue the options of color, scale-up, and commercialization of the FED technology. Additional work will be done with other companies to help define FED performance characteristics and display specifications. For further information, contact Sharron Bittick at Micron Display Technology at (208) 368-4400. *CA*

SUPERSET OF UTOPIA INTERFACE PROPOSED

A more highly defined interface protocol for asynchronous-transfer-mode (ATM) communication systems, called "SCI-PHY," was recently introduced to the ATM Forum for approval. The SCI-PHY protocol (Saturn Compliant Interface for ATM PHY devices) is intended to provide a complete standard for interconnection between the physical (PHY) layer and the ATM adaptation layer, or ATM layer devices. Created by PMC-Sierra Inc., Burnaby, B.C., Canada,, the protocol was developed with the Saturn ATM chip-development group to facilitate interoperability between manufacturers and further clarify the evolving ATM Forum specifications. The protocol is a superset of the Utopia interconnection scheme, which the ATM Forum accepted as an interoperability specification. Utopia limits its scope to defining logical and electrical timing between single ATM physical-layer devices and higher-layer functions. The Utopia interface doesn't provide support for interfacing multiple-PHY interfaces and isn't well defined enough to support higher data rates. The SCI-PHY protocol, designed for rates up to 622 Mbits/s, expands upon Utopia to support connections between the ATM layer and single or multiple physical-layer devices. To support latency management (critical for isochronous data), SCI-PHY also supports variable-length FIFO-status flag handshaking. To ensure interoperability, all SCI-PHY devices will be backward-compatible with Utopia interface-based products. For further information, contact Vern Little at (604) 668-7300. *LG*

IBM WORKSTATIONS RUN WINDOWS APPLICATIONS

The gap between Unix workstation platforms and Microsoft Windows applications will lessen even more with IBM Corp.'s (Armonk, N.Y.) introduction of the Wabi 1.1 for AIX. The interface, licensed to IBM by a division of Sun Microsystems, affords users of IBM RISC System/6000 workstations access to Windows-based applications, such as word processing, spreadsheets, and databases. Wabi 1.1 supports object linking and embedding, and dynamic data exchange (OLE/DDE) between Wabi-certified applications. On an RS/6000 Model 250 with 16 Mbytes of memory, performance of applications running under Wabi 1.1 is said to be comparable to that of some Intel 486-based PCs. *SVT*

INTERNET FORUM COVERS TEST SOFTWARE

Forums are being created on the Internet for just about any interest group these days. So why shouldn't there be one for test and measurement, particularly for people using National Instruments' LabView and LabWindows software? Users of the software are sponsoring and controlling the Info-Labview and Info-LW forums, which give them access to hundreds of other users. Anyone connected to the Internet can subscribe to user-sponsored mailing lists to discuss technical issues about LabView and LabWindows. The lists can be used to post technical questions about the software, or to suggest solutions to problems. National Instruments technical staff members monitor the forums and contribute information. To subscribe to Info-Labview, send your name and Internet address to: info-labview-request@pica.army.mil. Specify whether you want messages sent individually or in a daily digest format. Messages can be posted to the forum at: info-labview@pica.army.mil. To subscribe to Info-LW, send the message: subscribe info-lw <your name> to: listserv@tamvm1.tamu.edu. Messages to the group can be posted at: info-lw@tamvm1.tamu.edu. *JN*

Design delays taking thei

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	Altera FLEX	Typical Gate Array
Concept to Prototype	2 Weeks	6 – 10 Weeks
Up Front NRE Cost	No	Yes
Production Lead Time	Off the Shelf	8 – 12 Weeks
Reprogrammability	Yes	No
In-Circuit Reconfigurability	Yes	No
Flexibility for Design Changes	High	Low
Industry Standard CAE Support (VHDL, Verilog)	Yes	Yes

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MULTIPLE PROCESSORS SPEED VHDL SIMULATION

A multiprocessing simulation accelerator employs a mix of custom hardware and software techniques to speed all levels of VHDL descriptions. The Paradigm ViP accelerator, developed by Zycad Corp., Fremont, Calif., combines a native-code-compiled VHDL simulator, partitioning algorithms, and custom multiprocessing hardware. Each board consists of six MIPS R4000 processors running at 100 MHz, three custom ASICs for signal processing, and a custom I/O processor for communication with additional ViP boards and the host computer. There may be from 1 to 16 ViP processor boards installed in an accelerator system. This means that engineers can have from 6 to 96 R4000 processors working on one VHDL design simultaneously.

The R4000 processors provide parallelism to execute concurrent VHDL processes. The custom signal-coprocessor ASICs manage signal values, updates, and process wakeup. ViPSiM, the accelerator's software, analyzes VHDL code and generates MIPS object code to execute directly on the R4000 processors. Because the Paradigm hardware was created exclusively for VHDL, there's no operating-system overhead or external interrupts to slow the system down. Three user-selectable partitioning algorithms help divide the design among the processors. The Paradigm ViP accelerator is available now. Call (800) 243-7286 or (510) 623-4400 for more information. *LM*

MODELER ADDS BSIM3 FOR SUBMICRON DEVICES

BSIM3, the emerging standard for submicron device modeling, is now available in the Success modeling and device characterization tool developed by Anacad EES, Milpitas, Calif. The physical effects of deep submicron technology and the increasing complexity of circuits pose problems in the development of VLSI and ULSI designs. BSIM3 is a physical model, oriented to submicron MOSFET description. The BSIM3 model (unlike the process-oriented BSIM1 and BSIM2 models) contains a limited parameter set linked to physical phenomena. It thoroughly treats short-channel effects and can predict scaling effects on output characteristics before the process is ready. In addition, the model has extensive built-in dependencies of important dimensional and processing parameters, as well as major short-channel effects, such as threshold-voltage reduction. The Success modeling environment provides BSIM3 measurement, characterization, and optimization. Using Success with the BSIM3 model, engineers can analyze the implications and trade-offs of small MOS designs before committing to extensive manufacturing. For more information, call Anacad EES at (408) 954-0600. *LM*

SPANCEIVERS WILL MOVE DATA AT 200 MBYTES/S

The AutoBahn bus can operate without any latencies by increasing the data-transfer rate between system components, such as the CPU and memory. Until now, AutoBahn was merely a concept on the drawing board. Now, with the release of the Spanceiver transceiver chips, the AutoBahn is moving closer to reality. The chips, which come from a collaboration of Motorola Semiconductor and Pep Modular Computers, both out of Phoenix, Ariz., will eventually transfer data at 2.0 Gbytes/s. The first versions work on the VMEbus at 33, 50, or 100 Mbytes/s. Fabricated on Motorola's 0.8-μm Mosaic V process, the chip sits in a 14-mm-by-14-mm quad flat pack. The first applications for the AutoBahn technology will fall into wide-area networking, peripheral interfaces, supercomputing, fiber optics, and multimedia. For more information, call Pep at (602) 483-7100. *RN*

DISK FORMAT HIKES DATA CAPACITY BY 28%

A new formatting technique promises to boost the data capacity of hard-disk drives by 28%. Developed by scientists at IBM's Almaden Research Center, San Jose, Calif., the technique was made possible, in part, through the development of an advanced magnetoresistive-recording (MR) head design. The new design relies on a separate thin-film MR sensor for reading and an inductive element traditionally used just for writing. The high sensitivity of the MR element enables smaller bits and narrower tracks to be used, both of which increase areal density. Areal density is increased even further through the development of a "no-ID" sector format, which lends itself to faster, more reliable data writing and reading operations. In effect, the no-ID sector format works to raise data capacity by removing all of the disk-sector ID information that traditionally precedes every block of data. This function, no longer served by ID fields, can now be handled electronically, freeing up approximately 10-15% of the disk area to store more user data. Implementing both of these recent developments not only creates higher-capacity disk drives, but also increases high-performance MR-head manufacturing yields. The extra capacity is currently featured in IBM's latest line of magnetic hard-disk drives. This includes a pair of 810-Mbyte, three-disk models that contain 270 Mbytes on each 2.5-in.-diameter disk, specifically designed for use in laptop computers. For further information, contact Michael Ross of IBM at (408) 927-1283. *CA*

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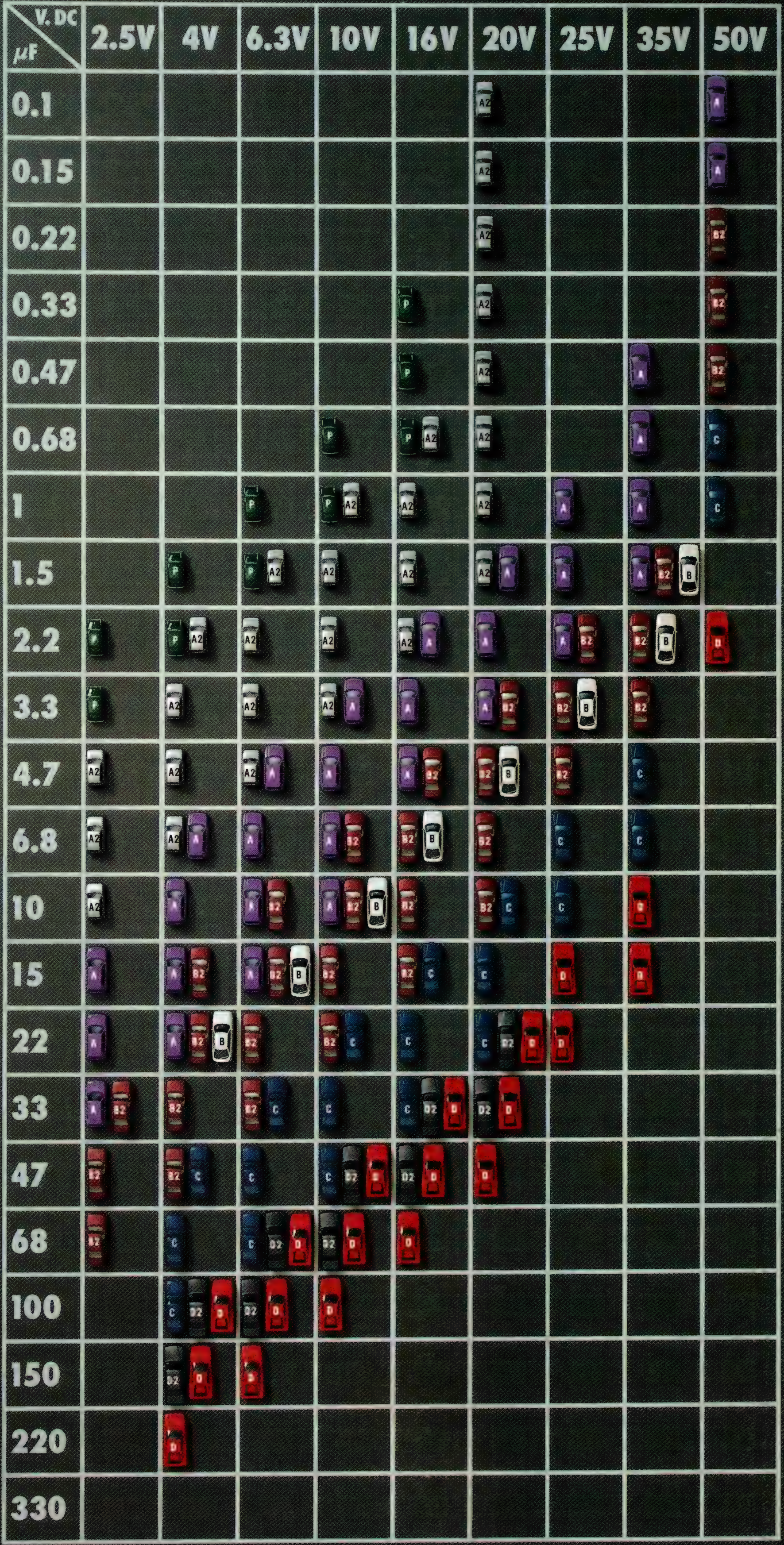
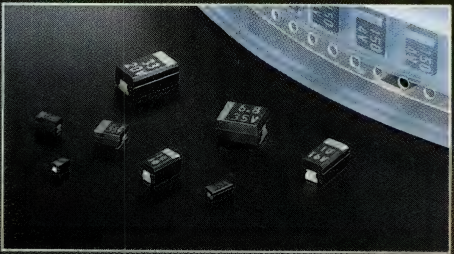
Case	L	W	H
P	2.0mm	1.25mm	1.2mm
A2	3.2	1.6	1.2
A	3.2	1.6	1.6
B2	3.5	2.8	1.9
B	4.7	2.6	2.1
C	6.0	3.2	2.5
D2	5.8	4.6	3.2
D	7.3	4.3	2.8



V. DC μF	2.5V	4V	6.3V	10V	16V	20V	25V	35V	50V
0.1						A2			A
0.15						A2			A
0.22						A2			B2
0.33					P	A2			B2
0.47					P	A2		A	B2
0.68				P	P A2	A2		A	C
1			P	P A2	A2	A2	A	A	C
1.5		P	P A2	A2	A2	A2 A	A	A B2 B	
2.2	P	P A2	A2	A2	A2 A	A	A B2	B2 B	D
3.3	P	A2	A2	A2 A	A	A B2	B2 B	B2	
4.7	A2	A2	A2 A	A	A B2	B2 B	B2	C	
6.8	A2	A2 A	A	A B2	B2 B	B2	C	C	
10	A2	A	A B2	A B2 B	B2	B2 C	C	D	
15	A	A B2	A B2 B	B2	B2 C	C	D	D	
22	A	A B2 B	B2	B2 C	C	C D2 D	D		
33	A B2	B2	B2 C	C	C D2 D	D2 D			
47	B2	B2 C	C	C D2 D	D2 D	D			
68	B2	C	C D2 D	D2 D	D				
100		C D2 D	D2 D	D					
150		D2 D	D						
220		D							
330									



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READER SERVICE 163

SID MEETING HIGHLIGHTS FLAT-PANEL ADVANCES...

The Society for Information Display (SID) Conference returns again this year, June 12-17 at the San Jose Convention Center in California, spotlighting the recent interest in advanced display technologies, particularly flat-panel displays. Many of the display technologies discussed at the SID meeting, developed in conjunction with government funding, are being directed at new mass-market opportunities like portable computers and high-definition television (HDTV). With over 230 technical papers, the SID Conference touches upon every imaginable aspect of how to improve current display technologies. Standout technical presentations include discussions on liquid-crystal displays (LCDs), electroluminescent (EL) displays, and field-emission displays (FEDs). *CA*

...IN LIQUID-CRYSTAL DISPLAYS...

In the realm of LCDs, scientists at Casio Computer Co., Ltd., Tokyo, Japan, recently demonstrated a 1.8-in. prototype ferroelectric LCD that can display a full-color motion picture of 220 by 280 dots. Because the flat panel uses a deformed-helix thin-film-transistor (TFT) process, it rubs only one side of the substrate on which a TFT is formed. The result is a much simplified cell-manufacturing process. Also, by implementing a driving scheme that relies on bipolar reset pulses and source-drain electrodes, the display exhibits excellent gray-scale characteristics and a wide viewing angle, surpassing the capabilities of current LCDs.

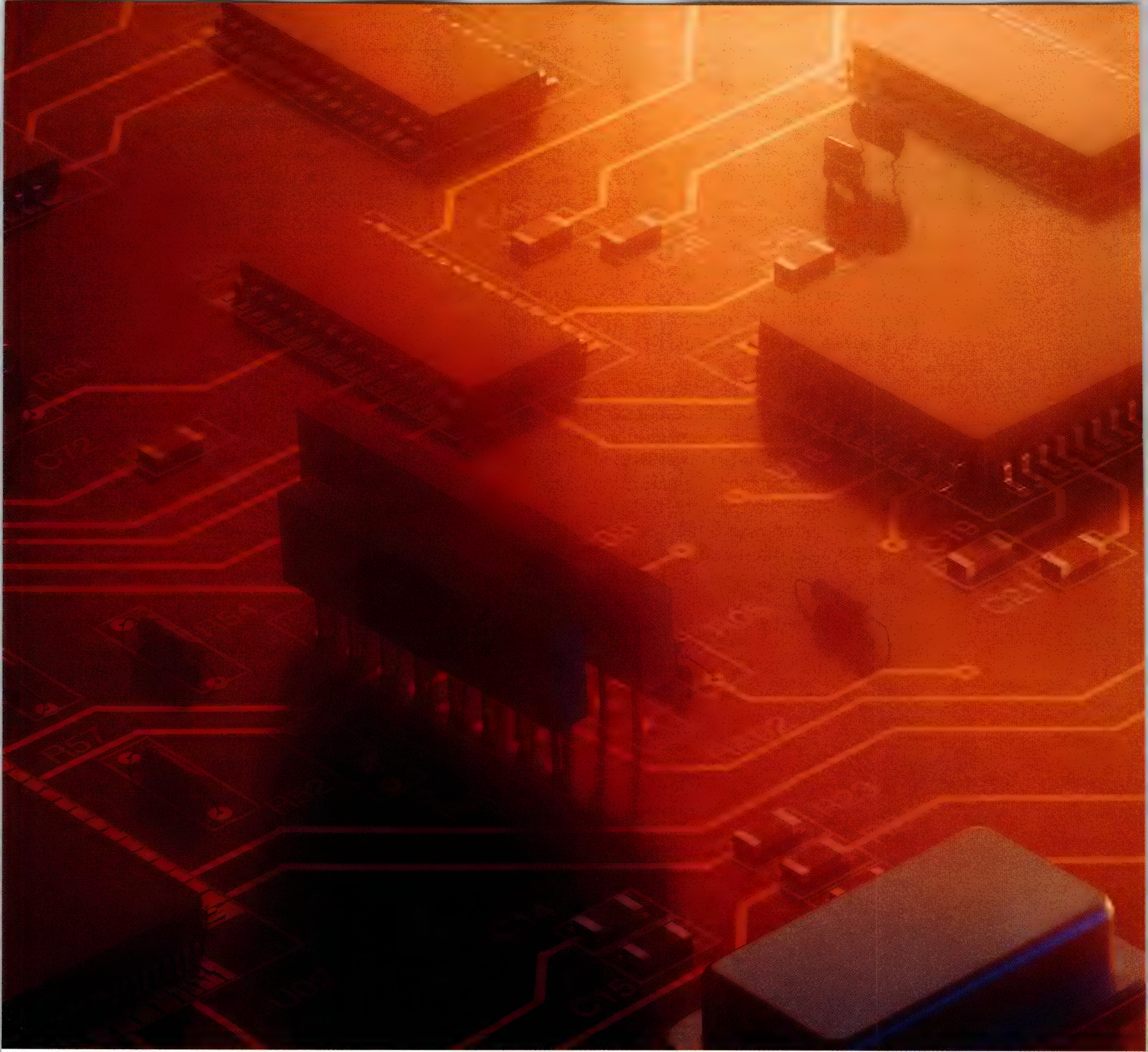
In the new display, composite-video signals are sent to a control circuit that separates synchronizing and video signals. The digitally-translated video signal is written into the memory as image data. Here, the data is translated to a driving scheme with the help of a second control circuit and transmitted to the data drivers fabricated by a tape-automated-bonding (TAB) method. The prototype display not only displays a TV broadcast, but due to its wide viewing angle, is watchable from any angle without having to reverse colors. Contact Casio at 0426-44-6113 for further information.

LCDs have made significant strides as flat panels, but one problem has been the development of practical large-area LCDs to compete with conventional CRTs. Scientists at the Mitsubishi Electric Corp., in Hyogo and Kyoto, Japan, think they've come up with an answer. They developed a 45-in. rear projector using a 350,000-pixel polymer-dispersed LCD panel whose resolution equals that of a CRT used for TVs. The actual display area has a 71.28-mm diagonal. It measures 56.7 by 43.2 mm and features 480 by 720 pixels. To obtain high screen brightness, the display relies on polysilicon material for the TFT elements in the LCD panel, scattering-type liquid crystals, and a high-aperture-ratio black mask. It features a specially-designed optical system for rear projection of the panel. An optical system generates highly collimated light that eliminates scattered light rays. This optical system was developed using a dichroic prism and a wide-projection-angle lens, and effectively incorporates a bent mirror and an aperture to eliminate any scattered light. Maximum screen brightness is 760 cd/m^2. Future developments will focus on ways to improve display contrast. For more information, call the Materials and Electronic Devices Lab of Mitsubishi Electric Corporation at (06) 497-7666. *CA*

...FIELD-EMISSION DISPLAYS...

FEDs are another hot and promising area for flat panels. A collaborative effort between SI Diamond Technology, Houston, Texas, and the Microelectronics and Computer Corporation of Austin, Texas, demonstrated that nanocrystalline diamond films fabricated by a laser-ablation process act as excellent field emitters. With this information, the companies developed a fully functional, monochrome 125-by-125-pixel matrix display. While the uniformity of diamond allows for almost all of the pixels to work, the researchers discovered that by increasing the number of emission sites per pixel—for example, from 5 to 10 emissions per pixel to over 50—a very uniform display could be obtained. Further testing showed that by integrating this uniform FED technology with various fabrication methods, low-cost, large-area matrix displays of up to 2500 by 2500 lines could be built. Continuing work in this area suggests that certain architectures will allow these diode-matrix displays to be driven with lower-voltage drivers than the full anode-cathode voltage. To obtain additional information, contact Dr. Nalin Kumar of SI Diamond Technology at (512) 250-2895.

To combine the high luminance and resolution of a CRT with the distortion-free image capability of a flat-panel display, Matsushita Electrical Industrial Co. Ltd., Osaka, Japan, developed a 14-in. color flat-panel display that's operated by multiple electron beams emitted from 44 cathode filaments. Dubbed Flat Vision, the display has an overall screen dimension of 272 by 202 mm and a 339-mm diagonal. It's also light, weighing in at a mere 7.9 kg. The display area consists of 442 by 440 pixels that emit a luminance value of 580 cd/m^2, and have a resolution of 340 television lines.



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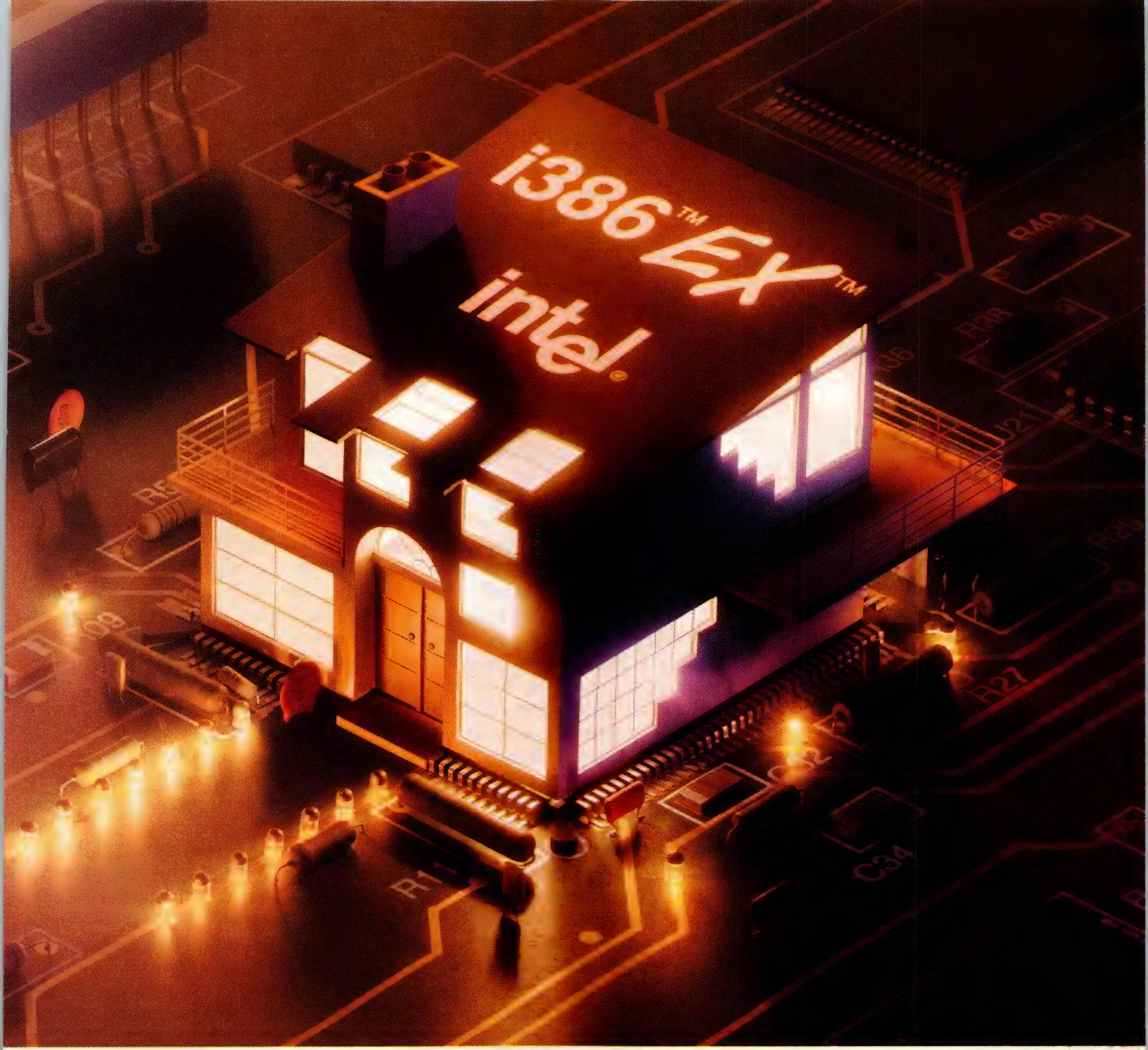

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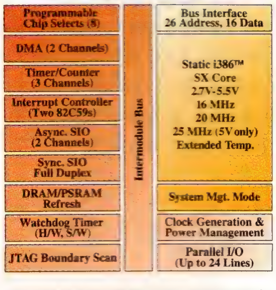
Embedded Intel386™ EX Processor Block Diagram


Programmable Chip Selects (8)
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Async. SIO (2 Channels)
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JTAG Boundary Scan
Intermodule Bus
Bus Interface 26 Address, 16 Data
Static i386™ SX Core 2.7V-5.5V 16 MHz 20 MHz 25 MHz (5V only) Extended Temp.
System Mgt. Mode
Clock Generation & Power Management
Parallel I/O (Up to 24 Lines)

CIRCLE 106 FOR U.S. RESPONSE

CIRCLE 175 FOR RESPONSE OUTSIDE THE U.S.

A major part of the development project focused on devising a means to secure a uniform picture from the discontinuities of raster created by the 44 filaments. To accomplish this feat, a picture-quality correction system was designed to take luminance information obtained by a camera, and correct the raster positions so that the luminances would be uniform. From this data, correction coefficients could be calculated by using a personal computer and subsequently be input into a correction block. The red, green, and blue signals, modulated by the correction coefficients, would then show a uniform picture on the screen. Using these techniques, developed to improve picture uniformity, the Flat Vision display achieves a picture quality rivaling that of a conventional TV CRT. For additional information, contact Keisuke Yamamoto, director of Matsushita Electric, at 0726-24-7730. *CA*

...ELECTROLUMINESCENT DISPLAYS...

EL displays represent another hotbed of activity in the world of flat panels. One advance comes from a four-way cooperative effort by Planar Systems, Beaverton, Ore.; the David Sarnoff Research Center, Princeton, N.J.; Allied Signal Aerospace Corp., Columbia, Md.; and Kopin Corp., Taunton, Mass. They fabricated an active-matrix zinc-sulfide:terbium (ZnS:Tb) green-emitting EL display with a resolution of 1000 lines per inch on a single-crystal silicon-on-insulator (SOI) substrate. The fully addressable flat-panel display contains 128 by 128 pixels. It combines high-frequency addressing circuitry with a high-resolution capability. These characteristics are made possible thanks in part to the SOI substrate, which allows the high-voltage transistors required for EL operation to be used. Researchers also discovered that by optimizing SOI-layer thicknesses and doping, the proper breakdown voltages and isolation capabilities that are also required for EL operation could be achieved. In addition, by using single-crystal silicon for IC formation, high-speed circuits needed for the peripheral shift registers and line drivers could be easily fabricated using standard IC-processing techniques. Specific characteristics of the active-matrix EL display include a thickness of less than 2 mm, high brightness, and low power. These characteristics make it ideal for head-mounted-display applications. Ongoing research will examine the feasibility of using this technology for other future innovative products. For more information, contact Planar Systems at (503) 690-1100.

The key to reducing the thickness of a flat panel is to replace the driver with a monolithic IC, according to scientists at the Texas Instruments Design Center in Tokyo, Japan. However, developing cathode-driver ICs that aren't plagued with problems associated with power dissipation and yet still satisfy the requirements of a color-panel pulse-memory driving method isn't as easy as it sounds. The solution, they found, was to create a new driving system based on a dielectric-isolation (DI) process that consists of an output circuit divided into two parts. One part was included in the IC, while the other was made up of discrete parts. In this manner, most of the power could be consumed by the outside of the IC. Test results showed that this output circuit allowed for a significant reduction in total power consumption, down to 2.4 W. A subsequent result of this study led to the development of two ICs—a 32-channel cathode driver and a 64-channel anode driver—specfically for use with a 26-in. color dc-plasma display panel application. Future evaluation will look into the possibility of using the driver ICs in displays reaching up to 40 inches. For further information, call the Design Center of Texas Instruments Japan Limited at 3-3769-8942. *CA*

...AND IN GLASS TECHNOLOGY

Progress in materials also is vital to the development of advanced flat-panel displays. To that end, the development of an innovative glass substrate for advanced flat-panel-display applications has been the focus of a study conducted by the Corning Inc.'s Technology Group, which has offices in Corning, N.Y., and Shizuoka, Japan. Fabricated using the fusion method, the substrate features a strain point of 666°C, low thermal shrinkage at both amorphous-semiconductor and polysilicon processing temperatures, chemical durability, and a low thermal coefficient of expansion. The substrate was originally developed for advanced active-matrix LCDs, but its characterization pushes the limit of what's offered by current commercial substrates, making it ideal for other applications, such as silicon microtip FEDs. With the glass material's inherent design flexibility, allotted by its enhanced chemical durability, any number of applications could stand to benefit from the newly developed 1737 glass substrate. Future studies will investigate these possibilities. For more information, call Corning at (607) 974-3527. *CA*

ALL FOR PAPERS

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Electronic Design is soliciting technical papers to be presented at the Portable By Design Conference February 15-17,1995 in the Santa Clara Convention Center, Santa Clara, Calif.

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To participate, respond to this call for papers by sending a one-paragraph abstract of a paper you would like to present. Papers should be oriented toward solving specific design problems.

Abstracts should be sent to: *Program Chair, Portable By Design* Conference, c/o Electronic Design Magazine, P.O. Box 821, Hasbrouck Heights, NJ 07604. Or, send by fax to (201) 393-0204.

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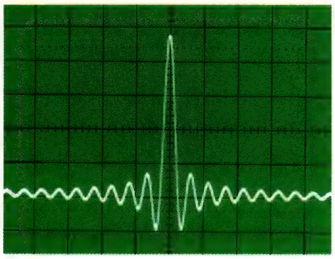

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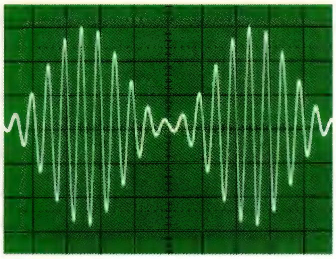

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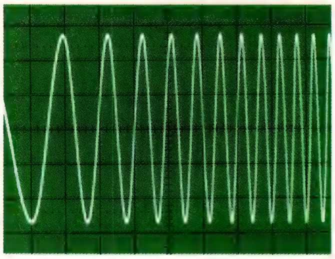

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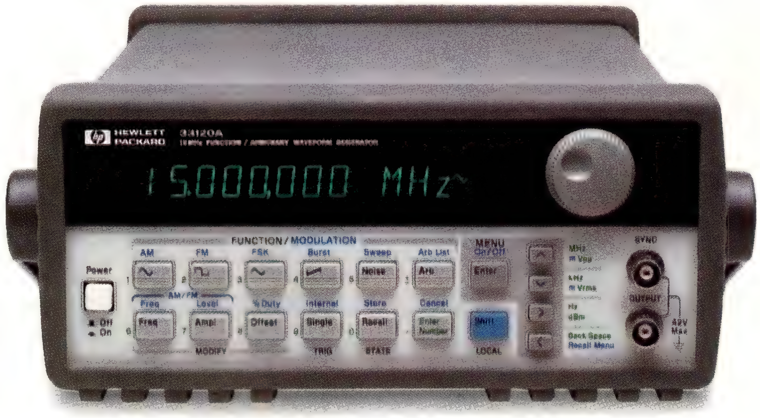

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IEEE Plans To Unveil A Low-Cost High-Performance Serial Interface With Speed And Flexibility

For computer-peripheral designers, an innovative low-cost and high-performance serial bus is on the horizon. It promises to offer a simple yet cost-effective technology for moving high-speed data between computers and peripherals, such as disk drives, video cameras, CD ROMs, printers, as well as audio and stereo equipment. "FireWire" has been designated by the Institute for Electrical and Electronic Engineers (IEEE) as the P1394 standard, and will be released this year.

The P1394 serial bus, developed by the Apple Computer Corp., Cupertino, Calif., employs six wires (two are used for data, two for strobe signals, and two for power) to provide users with a choice of three data-transmission rates of 100, 200, or 400 Mbits/s. It can handle as many as 63 devices at up to 72 m.

The P1394 bus architecture automatically configures itself at the power-up stage and permits "hot plugging" (the addition and removal of devices from the bus while power is on). In addition, it can transmit both asynchronous as well as isochronous data types. FireWire is the product of a collaboration between several companies that include Adaptec, Apple Computer, IBM, Maxtor, NCR, Texas Instruments, and Western Digital.

Heightened interest in FireWire can be seen in both the industrial and consumer markets. It suits applications such as automotive data buses and can serve as a standard interface between audio and video components *(see the figure)*. Its ability to transmit isochronous data also make it an ideal candidate for various multimedia applications.

Mike Salas, FireWire product program manager at Texas Instruments, Dallas, is excited about the potential implications of the technology. "It's the next big interface to emerge in the computer industry," says Salas. He explains that the P1394 bus' speed and flexibility will provide designers with a technology to bridge the consumer, industrial, and computing worlds.

At the physical level, FireWire is a serial bus that employs both a data and strobe channel. Each channel is connected to a separate twisted-pair shielded wire via a differential driver circuit that swings within 200 mV p-p. Because the strobe signal is designed to transition during any period that the data does not, a data clock is synthesized from the XORing of the two signals. The third pair of wires provides 8 to 40 V of user-defined power to the peripherals, allowing the transceiver circuits to be operational, regardless of whether a unit is turned on or off. This bus power also can be used to operate low-power peripherals.

Each FireWire node is self-configuring, assigning itself a unique node identification number upon power-up. A hot-plugged node automatically takes the next available ID code for itself.

Communication between nodes occurs in variable-length packets that are sized in multiples of 4 bytes or quadlets. Contention for the bus is handled by the "root" node using a fair arbitration scheme. The root node is the device possessing the lowest-node ID code.

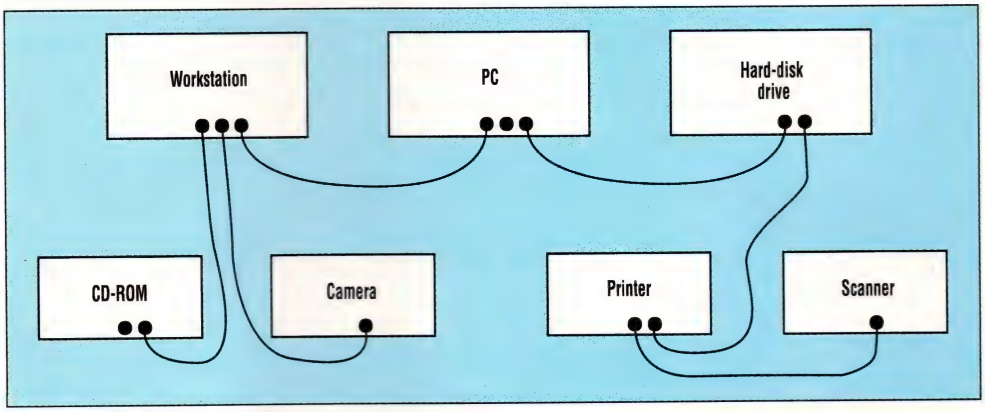
During a transfer cycle, the root node polls each node sequentially and gives it control over the bus if its Arbitration Enable flag is set. Once finished with the transfer process, a node resets its Arbitration Enable flag and can't access the bus again until the next cycle.

Communication is accomplished through five types of packets: quadlet, block, isochronous, no-data, and acknowledge. Data is transferred using block or isochronous packets, while intra-node signaling is usually performed using the shorter quadlet and no-data packets.

The acknowledge packet, which is a single-byte message used to confirm a packet transfer, contains a 4-bit receiver status code and a 4-bit parity check. Block packets are used for asynchronous data transfers and have a maximum length of 512 bytes, while isochronous packets may be up to 1024 bytes in length. The protocol within the P1394 standard allows up to 32 isochronous communications channels to be established within the network's bandwidth.

The FireWire interface is moderately intelligent and can offload much of the work of peripheral management usually performed by the CPU within the host-computer system. By using the P1394 bus, host-computer devices can communicate with peripherals via a standard command set called the serial bus protocol (SBP). The SBP commands direct the interface, which in turn performs the transaction with no further supervision, freeing up the host computer for other tasks.

With FireWire's official IEEE approval anticipated for later this year, Texas Instruments already has introduced the first silicon de-



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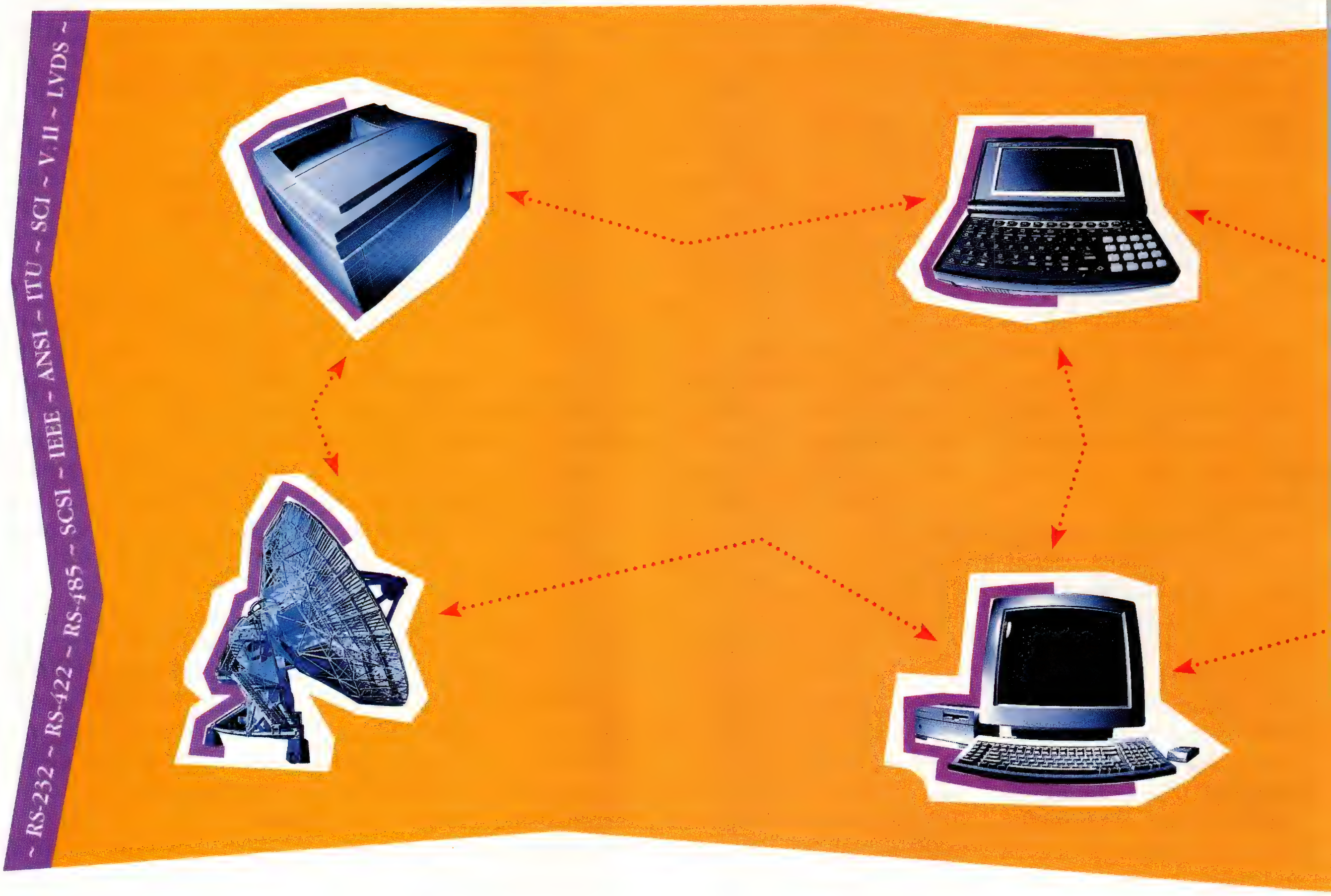
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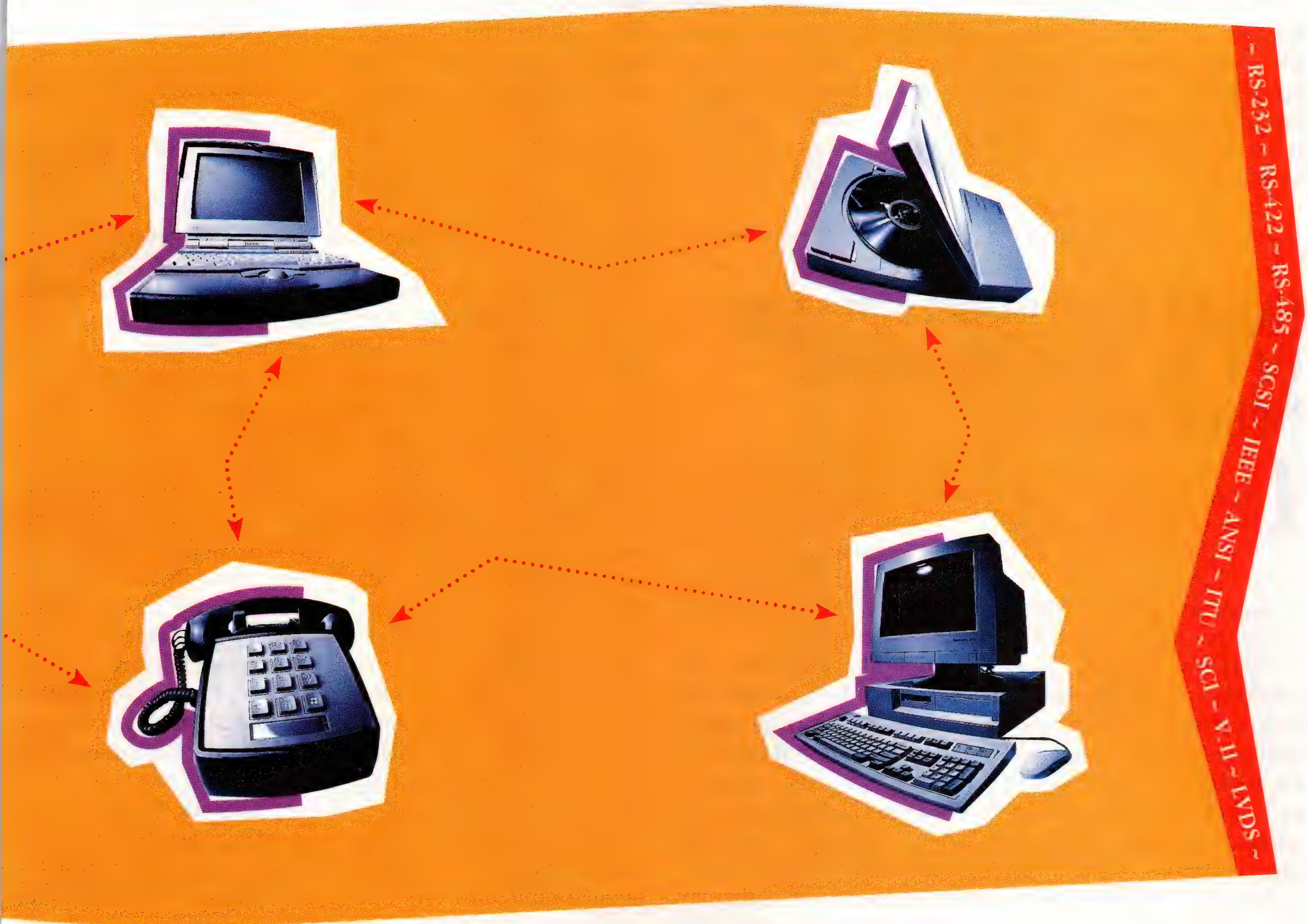
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vices that support the new interface. The two-chip set provides both a physical-layer and a link-layer interface.

The physical layer is supported by a mixed-signal chip that contains three transceiver nodes and the bus-arbitration logic to drive them. The multiple transceivers provide a host system with three independent channels for such applications as disk-storage devices, printers, and intra-computer data communications.

The link-layer chip contains the error-checking logic, a set of FIFO buffers, and a 32-bit general-purpose host-computer interface.

The two-chip set will be introduced in a 100-Mbit/s version. Later releases of the chip set will support 200- and 400-Mbit/s data-transfer rates.

The initial pricing of the chip set will be under $45. Texas Instruments feels that at such a low price, FireWire can serve as a low-cost, high-performance standards-based interface for applications in which circuit board and connector space is limited.

LEE GOLDBERG

SMART BATTERIES SPELLED OUT BY JOINT ENABLING SPECIFICATION

It's an all-too-common occurrence for the portable-computer user: On a cross-country flight, say, over Kansas, your PC crashes and your work-in-progress is lost when the computer's battery pack breathes its last. Maybe you forgot to fully recharge the batteries before you left. Or, perhaps, you fell victim to one of the numerous inadequate methods of gauging battery voltage. In either case, without warning, you're sunk.

In an effort to make this scenario a thing of the past and to further its goal of coming up with standardized battery packs, Duracell International Inc., of Bethel, Conn., teamed with Intel Architectural Labs, of Beaverton, Ore., to establish two specifications for the creation of smart and rechargeable batteries. Duracell hopes that its smart batteries will combat the dead-in-flight PC problem on two fronts: One, they'll increase computer run times, and two, they'll help to institute a new design standard for future generations of portables, including highly accurate state-of-charge feedback and display.

Generally, batteries and their host devices function in a master-slave arrangement. The host device dictates its power requirements to the batteries, and when power demands swell, such as when a hard disk spins up or a display backlight is turned on, the host simply increases its current draw and the battery complies—if it can.

"Smart" batteries are battery packs equipped with specialized hardware that informs their host of their present state of charge, and calculated and predicted run time. This capability will give users an accurate prediction of remaining operating time. Instead of the master-slave relationship, the battery becomes an interactive partner in power management by informing the host computer and user that it either is or isn't up to the task at hand.

The standards cooked up by Duracell and Intel address two key aspects of smart batteries: the information and protocol, and the physical pathway for that data. The Smart Battery Data (SBD) specification defines the data that flows between the smart battery, its host, and other devices. The specification is generic with respect to the type of battery chemistry and the battery-pack voltage, capacity, and physical packaging.

The second specification defines the System Management Bus (SMBus) and describes a simple protocol for communication taking place between power-related devices. Through the specification, a system can provide control to a smart battery or batteries, a smart-battery charger, and various regulators and switches. Each device has a standard slave address and exchanges its information through a specific command set. A specification for a smart-battery charger is forthcoming.

The batteries themselves, along with the intelligence built into them, lie at the heart of the smart-battery scheme. The packs, which will be updated versions of Duracell's existing standardized nickel-metal-hydride (NiMH) packs, will contain an ASIC programmed with 34 distinct parameters for self-diagnosis. These include battery current, state of charge, remaining run time, alarms, and device and brand identification data. The small, low-power ASIC carries a reference library of proprietary battery information that gives it a means of gauging the packs' condition. The packs themselves will incorporate a fuel gauge and communicate charge information to the host device for display.

Duracell has enlisted significant industry support for the new specification. Compaq Computer Corp., which already employs Duracell's NiMH packs in its new Contura Aero subnotebooks, has given the specification its blessing. In addition, BIOS vendors Phoenix Technologies and SystemSoft are both developing products to support the specifications. Furthermore, various component suppliers that have signed on include ACC Micro, Maxim Integrated Technologies, Opti, PicoPower, and VLSI Technologies Corp.

Smart batteries aren't limited to computers, nor are they limited to the NiMH chemistry. Duracell is adapting its four existing standardized NiMH packs (for PCs and camcorders) to the new smart-battery scheme. The battery maker will next turn its attention to cellular telephones. The battery-intelligence scheme is readily adaptable to other chemistries, including emerging technologies such as lithium ion. The smart batteries will be shown at this fall's Comdex show (Nov. 14-18, Las Vegas, Nev.), at which time Duracell will divulge how much the technology will add to the cost of rechargeables.

For copies of the SBD and SMBus specifications or for additional information, call a local Intel sales office at (800) 626-7256 or its Literature Center at (800) 253-3696. You also can contact Duracell at (800) 422-9001, ext. 423.

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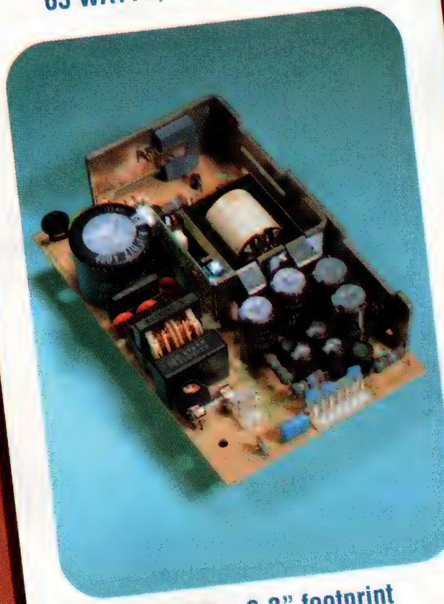

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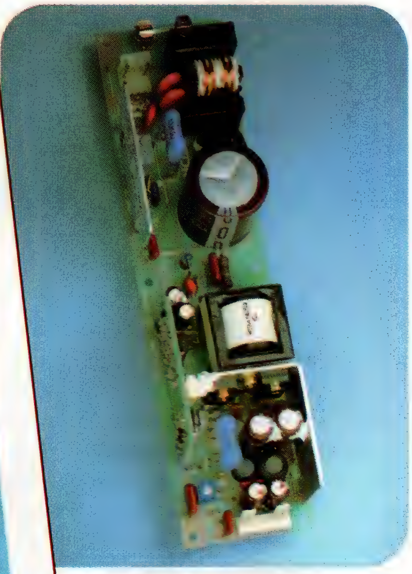

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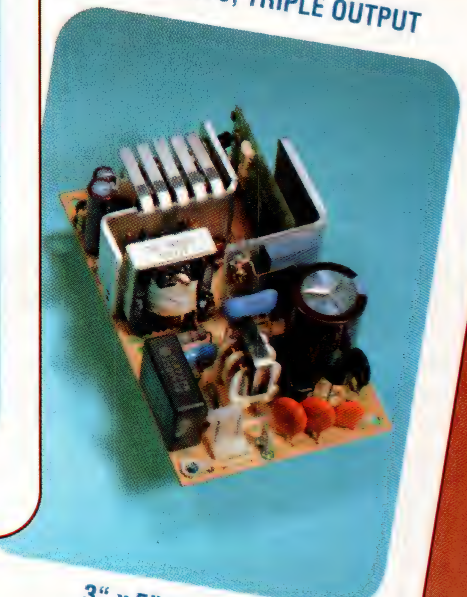

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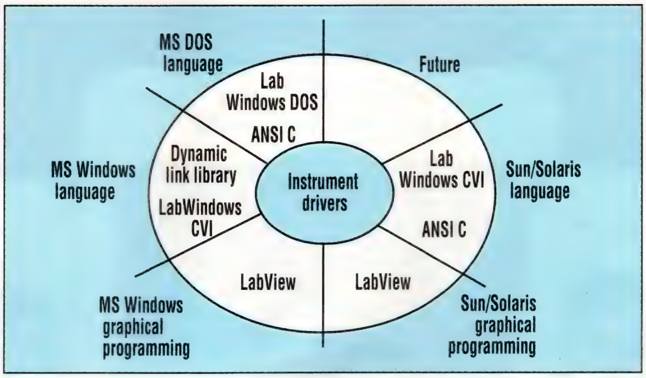
VXI SYSTEMS ALLIANCE GROUP RELEASES STANDARDS FOR BUILDING MULTIVENDOR INSTRUMENT SYSTEMS

The first four specification documents have been released by the VXIplug&play Systems Alliance. The new documents are aimed at easing the task of integrating VXIbus components from different vendors. The specifications describe how to design, code, install, and distribute standardized instrument drivers, soft panels, and installation disk drives.

The Systems Alliance notes that these first documents standardize core specifications needed to create and use multivendor VXI systems. In the past, numerous software operating systems and low-level drivers for VXI products caused high-level programming differences for devices from different equipment vendors, the group says. In addition, end-users have been very vocal in their complaints about the difficulty in making systems from multivendors work.

The first four documents, which are open and available to anyone, include:

- *VPP-1, the Charter Document.* This document discusses the group's guiding principles and explains how the Systems Alliance is accommodating all established standards, both formal and de facto. It also shows how the group is building frameworks to maximize software reuse and to simplify development of multivendor systems.
- *VPP-2, the System Frameworks Specification.* This specification defines popular frameworks with easily recognizable names. It defines the system-level interfaces located within the frameworks and explains how users choose a framework as a foundation on which a system can be built. The frameworks are separated by hardware platforms, operating systems, and the programming style *(see the figure)*.



- *VPP-3.1, the Instrument Drivers Architecture and Design Specification.* This defines the modular architecture for all drivers. It also describes standards for on-line help, documentation, error handling, and revision control.
- *VPP-3.2, the Instrument Driver Developers Specification.* This specification contains guidelines for developing instrument drivers with a consistent look and feel. It has template functions for all drivers and example implementations for common instruments. It also features detailed steps of the development process to help users create drivers for use with standard languages.

Three other documents are in the works and should be voted on and completed in the coming months. The Installation and Packaging Specification will define a standard installation program for all VXIplug&play test and measurement instrument driver disks.

The Soft Front Panel Specification will describe guidelines for developing and packaging soft front panels to be shipped with test and measurement instruments. The concept of executable front panels, which developers can use immediately upon installation to verify that instruments are working properly, was a founding tenet of the Systems Alliance.

The final standard, the VISA (virtual instrument software architecture) I/O Software Specification, is a 400-page document currently in draft 2.0. This standard will define a software layer of I/O calls, interrupt handling, and data movement. It will give driver developers a standard platform on which to build the tools needed to use their test and measurement instruments.

The specification will be backward-compatible with all existing I/O drivers, including the NI-VXI and NI-488 drivers developed by National Instruments and the standard interface control language (SICL) developed by Hewlett-Packard. The document also will address the next-generation needs with an object-oriented architecture and distributed resource management.

The VXIplug&play Alliance was founded last September by several test and measurement instrument companies, including GenRad, National Instruments, Racal Instruments, Tektronix, and Wavetek. Its goal is to endorse and implement common system-level standards and practices beyond the scope of the baseline specifications produced by the VXI Consortium.

Membership has since grown to 17 organizations. A users group also was established by the alliance; any VXI user or potential user can join without cost. The group had 64 members as of last month.

For more information on the VXI Plug & Play Alliance, contact Ron Wolfe at National Instruments Co., Austin, Texas, at (512) 794-5466.

JOHN NOVELLINO

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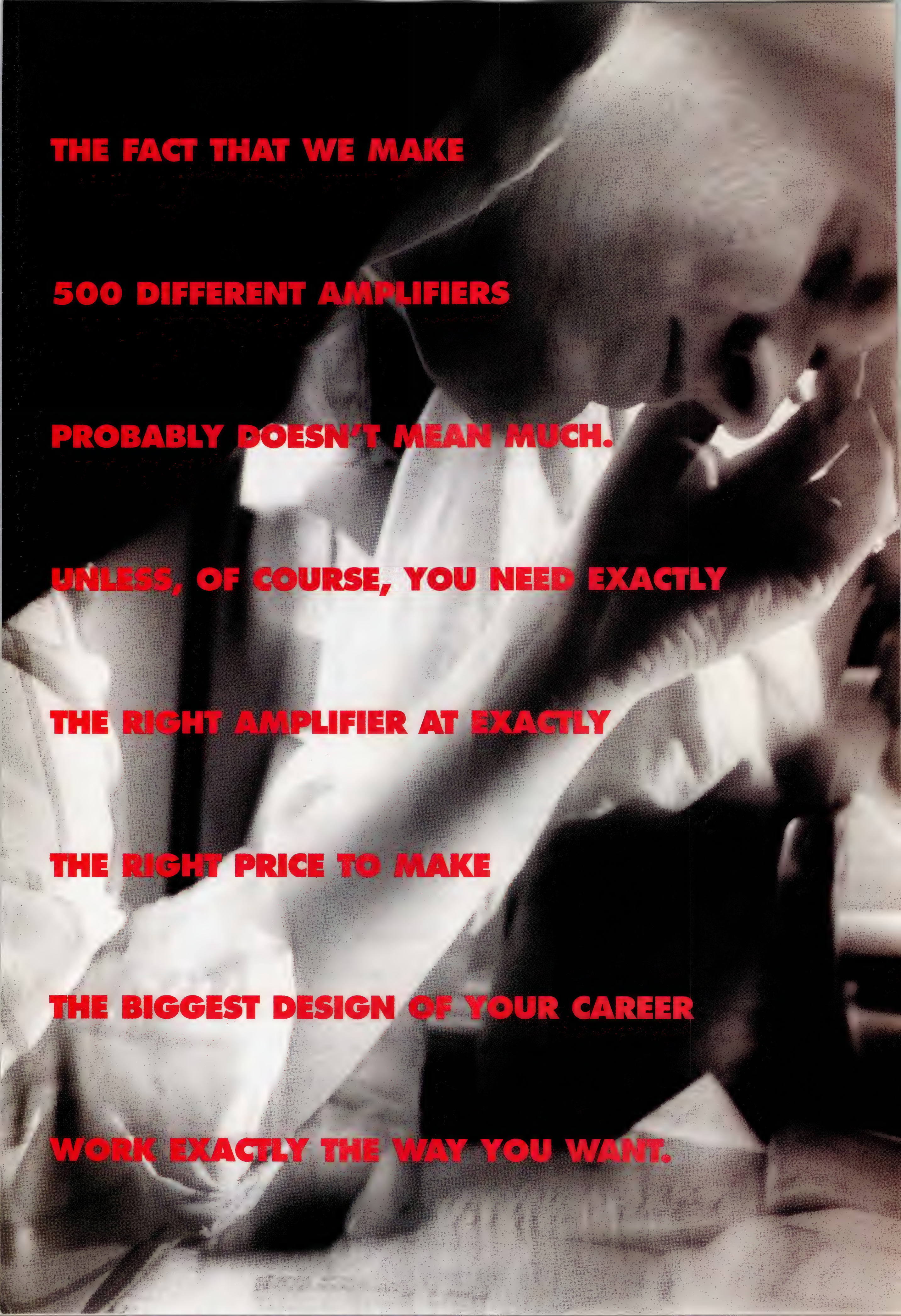
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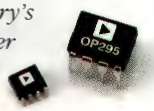

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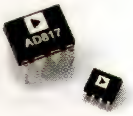

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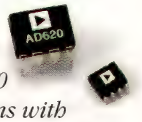

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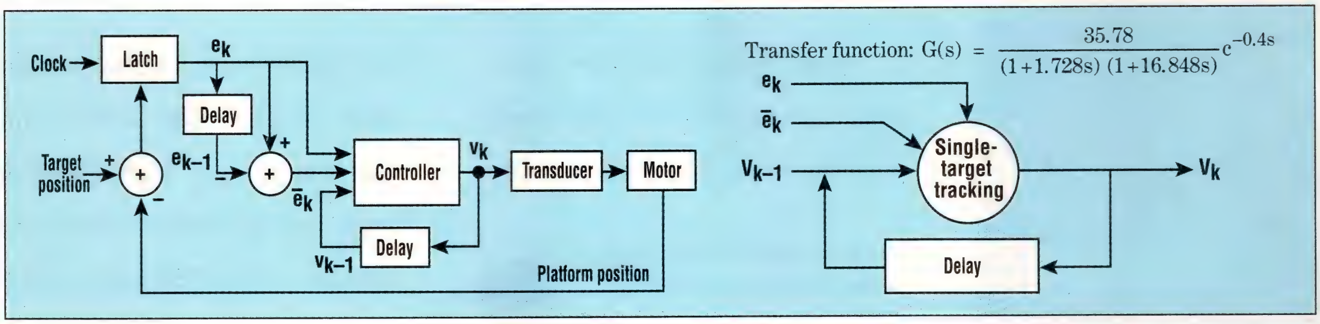

control rules. These rules are actually conditional linguistic statements that describe the process-control algorithm as a relationship between the input and the desired output for the process.

Armed with this information, researchers at Sensor Data Integration Inc., Concord, Mass., developed a fuzzy-logic controller to track a single non-maneuvering target. The circuit, which controls the speed of an automobile, was recently described at last month's Electro/94 International Conference in Boston, Mass.

The technique uses an inference module that describes the production rules based on a "condition" block (sometimes called an "antecedent" or "if" block) and a conclusion block (also called the "consequent" or "then" block). The output is derived from the sum of the inferences.

In the automobile-controller design, a set-point value, s, is fed into a microcomputer and converted to an analog signal by an digital-to-analog converter, all within the fuzzy-logic controller. This signal is next fed to an external final-control element that manages the automobile's speed. Then, the speed signal is fed back to the fuzzy-logic-controller circuit, whereupon it's digitized by an analog-to-digital converter and fed back to the microcomputer circuit.

The fuzzy-logic controller simplifies the tracking process by independently analyzing the target's azimuth and elevation movements. The controller's performance is optimized primarily for error and, to a lesser extent, for computation time. The resulting system is a multiple-input, single-output closed-loop proportional controller circuit with the platform drive-motor voltage representing the feedback variable.

The fuzzy-logic controller employs three input variables: e_k, $\bar{e}_k$, and V_{k-1}, and one output variable, V_k *(see the figure)*. It uses a unit-delay element in a closed loop from the output to feed back to its final input, which is the voltage that's applied to the platform servo motors.

Experimental results were summarized with heuristic rule-based learning programs and membership functions. The most significant improvements came from the enhanced rule-based learning.

The transfer function of the controlled system, G(s), including the final control element, was approximated from a step response. The circuit's speed-control behavior was found to be close to that of a human operator *(see the equation in the figure)*.

As the controlled variable (speed) gets close to the set point value, s, the speed value slows down slightly and then settles up at the set point. Such a response could not be realized using a conventional proportional/integral controller circuit.

The primary goal for this single-target, automotive-tracking fuzzy-logic controller is to demonstrate a reduced tracking error. The reduced error is derived using a rule-based learning program and compared with a Kalman filter-based tracker to demonstrate the reduction in error.

The controller assumes that a radar system supplies the target position with a 40-Hz sampling rate. The target position employs X-Y-Z Cartesian coordinates, which are then transformed into Alpha-Beta-range spherical coordinates for the controller. The linear trajectories, which are either constant-velocity or constant-acceleration values, move through Cartesian 3 spatial coordinates. However, the tracking software requires polar 2 spatial coordinates. The controller doesn't use the third dimension of the polar range.

For more information on the design of this fuzzy-logic controller, contact Sensor Data Integration, Concord, Mass., at (508) 369-7325.

RICHARD NASS

PACKAGING TECHNIQUE USES GLASS-ON-SILICON SUBSTRATE TO CARRY MICROWAVE ICS

Conventional plastic packages as well as printed-circuit boards perform poorly as signal operating frequencies climb into the microwave region. With information and communication technologies exploding into the commercial marketplace, microwave circuitry will be turning up virtually everywhere. But the alternatives to plastic and the FR-4 materials used in microwave circuits for the military are too expensive for high-volume commercial uses. Therefore, some creativity is called for when packaging these very-high-frequency circuits.

To that end, designers at the Microelectronics Division of M/A-COM Inc., Lowell, Mass., have come up with a capability called glass microwave-IC technology. The packaging technique allows for the integration of microwave ICs and discrete devices into a high-performance circuit

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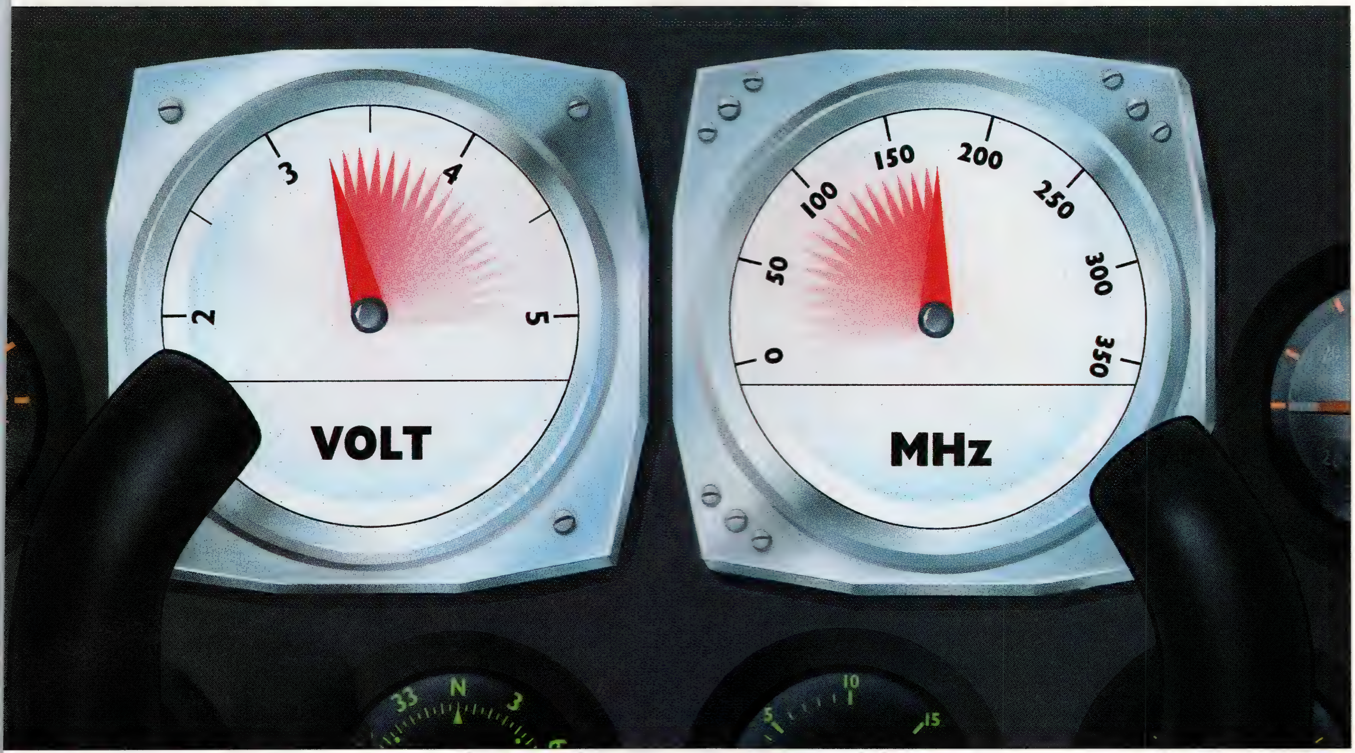

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medium that supports low-cost manufacturing. The technique was described last month at the Electro/94 International Conference in Boston, Mass.

In general, a microwave-circuit medium must provide accurate transmission-line impedance and low RF losses. The ability to fabricate passive components is desirable for integrating matching and bias networks on the same substrate.

To address these needs, researchers at M/A-COM developed a glass-on-silicon wafer as the base substrate for microwave circuits. Standard thin-film semiconductor fabrication techniques are employed to create the conductor patterns as well as other circuit elements.

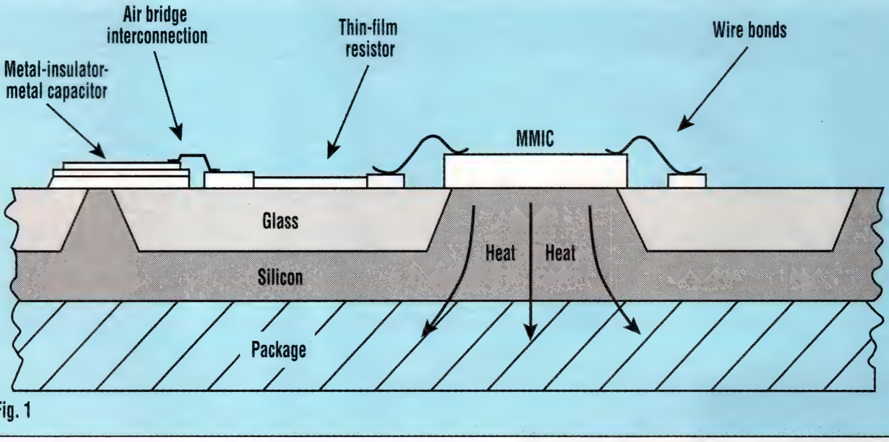

Fig. 1

The glass is a low-loss borosilicate material with a dielectric constant of 4.1. It features a loss tangent of 0.002 at a frequency of 10 GHz and serves as the microwave transmission medium *(Fig. 1)*.

The ground plane of the circuit is a layer of gold or silver at the glass-silicon interface. Ground can be brought to the surface by means of via structures in the 8-mil-thick glass. The heavily-doped silicon wafer provides a conductive interface between the ground layer under the glass and the final package. The resulting substrate, a planar wafer, supports nearly all of the standard production methods used by the semiconductor industry.

A very close match in the thermal coefficient of expansion is achieved between the glass and silicon materials, making for a reli-

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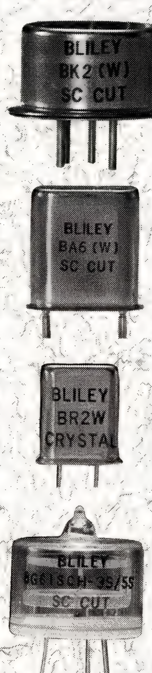

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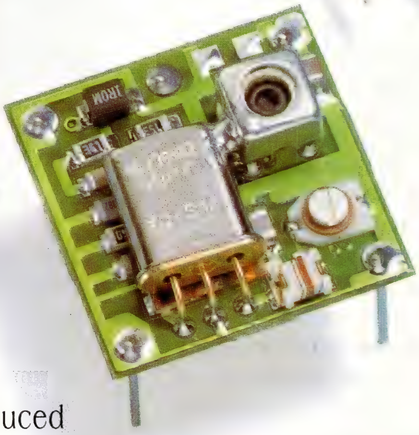
Crystal Components for Telecommunication Networks



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1.544	T-1 (DS 1)	T-1 (DS 1)	T-1 (DS 1)	T-1 (DS 1)	T-1 (DS 1)	–
12.352	T-1 (DS 1)	T-1 (DS 1)	T-1 (DS 1)	T-1 (DS 1)	T-1 (DS 1)	–
16.384	SDH SONET ISDN	SDH SONET ISDN	SDH SONET ISDN	SDH SONET ISDN	SDH SONET ISDN	SDH SONET ISDN
38.880	SDH/STM-1	SDH/STM-1	SDH/STM-1	SDH/STM-1	–	–
44.436	ATM T-3 (DS 3)	ATM T-3 (DS 3)	ATM T-3 (DS 3)	ATM T-3 (DS 3)	– –	– –
51.840	SONET/STS 1	SONET/STS 1	SONET/STS 1	SONET/STS 1	SONET/STS 1	–
155.520	ATM STM-1/STS-3c SONET/(OC-3c)	ATM STM-1/STS-3c SONET/(OC-3c)	ATM STM-1/STS-3c SONET/(OC-3c)	ATM STM-1/STS-3c SONET/(OC-3c)	– – –	– – –
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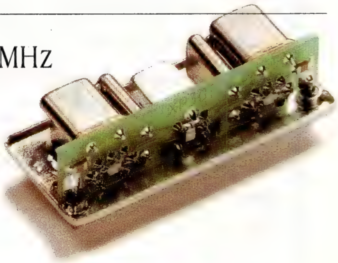

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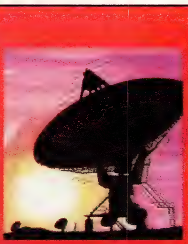

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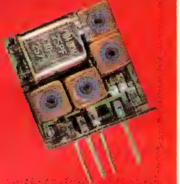

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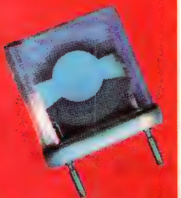

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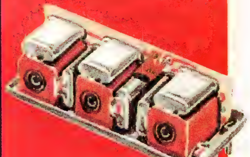

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able interface that supports processing at temperatures up to 800°C. In addition, the glass is easily polished to a defect-free surface for the fabrication of fine-line patterns and high-yield, thin-film, metal-insulator-metal (MIM) capacitors. Other circuit elements routinely fabricated during the wafer process include resistors, capacitors, spiral inductors, air bridges, couplers, and transmission lines *(Fig. 2)*.

Not only does the silicon wafer serve as a mechanical carrier for the thin glass layer, but it also provides zones of high thermal conductivity for mounting devices that generate heat. Completed wafers combine the low-loss attributes of glass with the favorable thermal characteristics and easy processing of silicon.

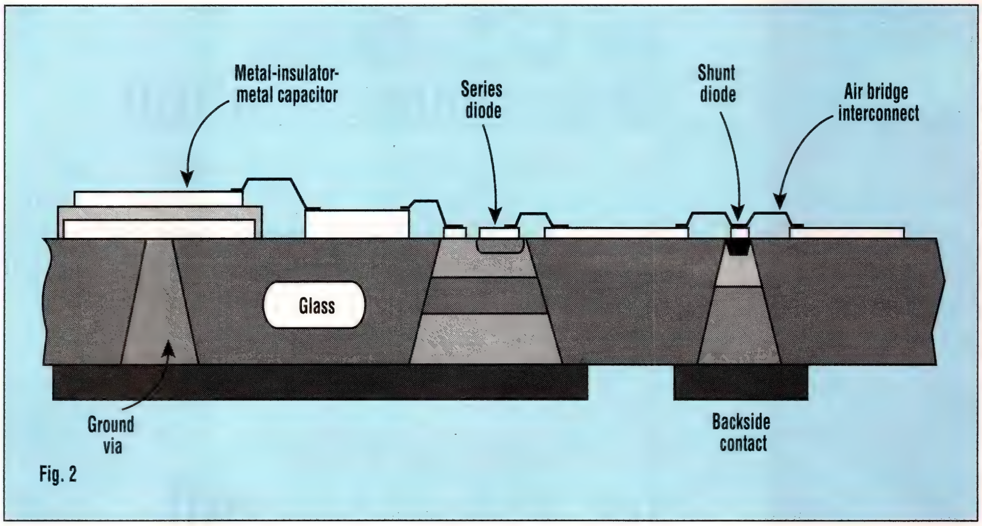

Fig. 2

While completed glass-silicon wafers contain all of the passive components typically used in microwave circuits, most applications still require the addition of various discrete semiconductors. A handy characteristic of the wafers is the ability to perform conventional or flip-chip assembly as well as dc and RF testing on the intact wafer rather than on individual substrates. This minimizes handling of the individual substrates and eliminates many of the problems related to test fixturing.

For more information on the packaging technology, contact M/A-COM at (508) 442-5000.

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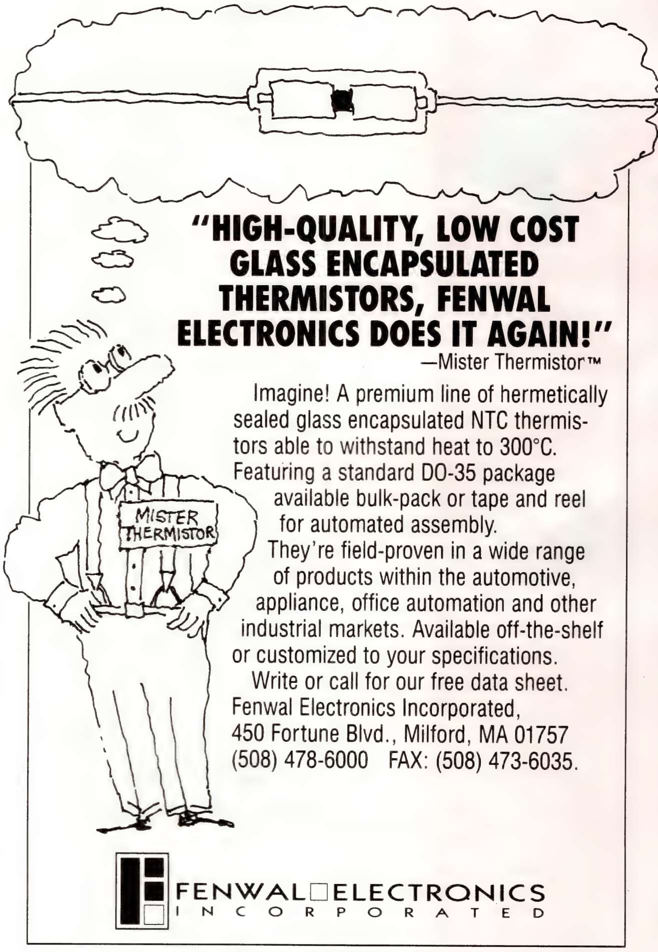

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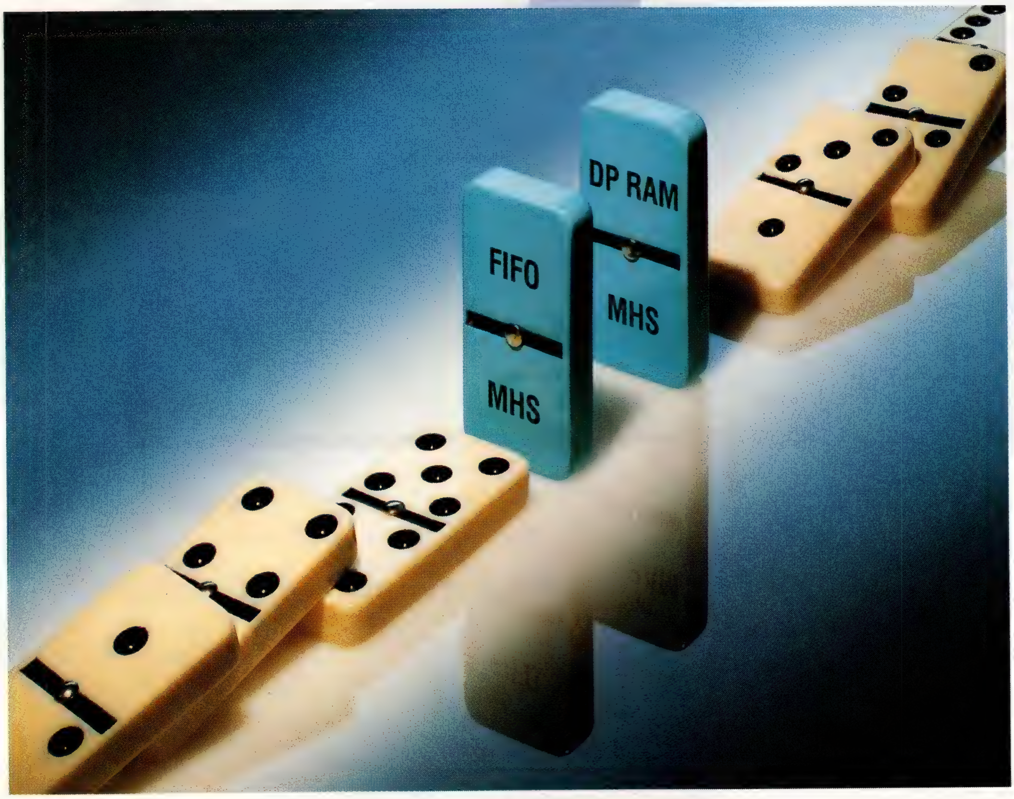

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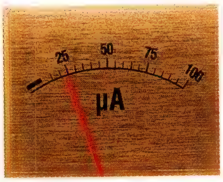

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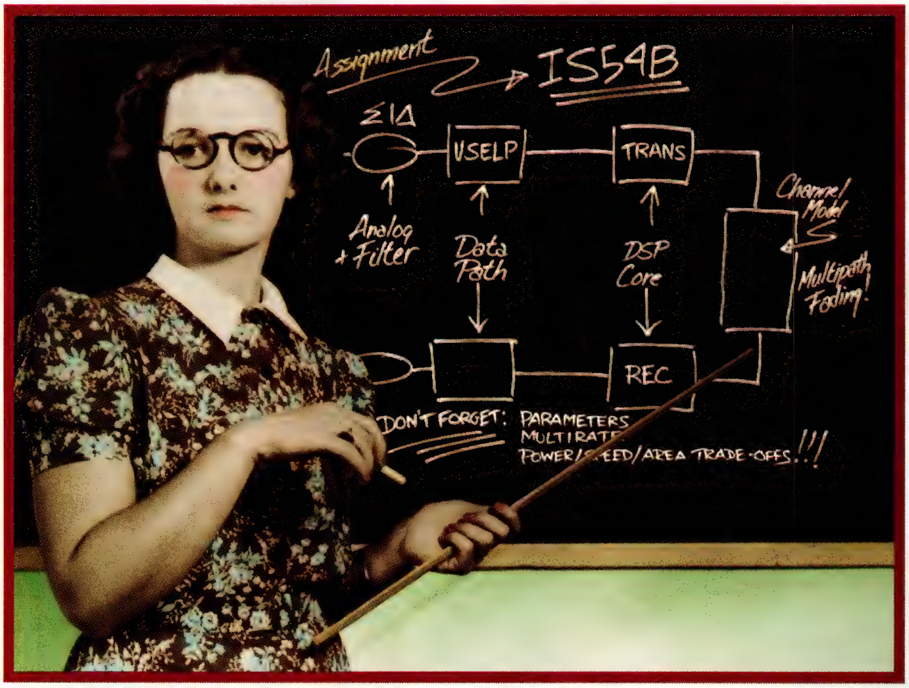

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MAC PROTOCOLS: THE KEY TO ROBUST WIRELESS SYSTEMS

A PREVIEW OF THE IEEE 802.11 MEDIA-ACCESS-CONTROL PROTOCOL GIVES INSIGHT INTO WIRELESS LANS.

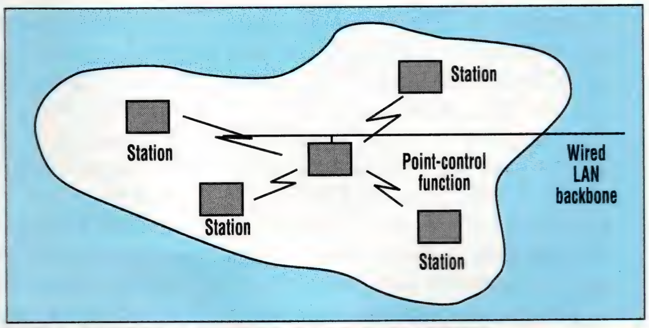
LEE GOLDBERG

As wireless devices move from specialty markets to becoming as ubiquitous as telephones, congestion in the finite electromagnetic spectrum is turning into a serious problem. More and more people are using wireless technology both at work and at home. Cellular-telephone use has grown to 14 million U.S. subscribers, and wireless terminals are helping retail and manufacturing operations rapidly collect and respond to critical information. Many field workers can be in constant contact with their home office via radio messaging units, and personal communication system (PCS) devices. One of the largest potential markets for wireless technology is the local-area-network environment. Adding wireless access to an existing LAN frees people from their desks, giving them access to information wherever they are working.

As the airwaves becomes more crowded, frequency management issues such as standards for data compression, frequency control and media access protocols have become hot topics in nearly every wireless application community. *(see "Standards wars in the wireless world," p. 66).* In response to the potential for gridlock in the airwaves, a new generation of sophisticated communications protocols is under development by standards committees such as the International Standards Organization European Telecom Standards Institute (ISO:ETSI) and the Institute for Electrical and Electronic Engineers (IEEE).

These new communications protocols contain new "rules of the road" designed to increase both the number of users and the amount of data that can be sent over the airwaves in a given area. To better understand the kinds of issues that any wireless protocol must address, we can examine the technical challenges which arise when adding wireless capability to the existing wired LAN technology.

Communications protocols reside in the lower layers of the ISO's seven-layer Open Systems Interconnection (OSI) reference model. It's the job of a media-access-control (MAC) protocol to provide the "glue" that binds network nodes together down at the physical layer



1. USING A POINT-COORDINATION function setup gives a node an access point to a local-area network. The node provides coordination and contention control for all stations within its jurisdiction.

(layer 1) and link layer (layer 2). At the physical layer,the IEEE has specified that either RF or infrared (IR) transmission may be employed.

For unlicensed networks, maximum RF transmission power is set at 1 W or less, but the small battery size of most portable devices usually keeps power down to 1-or-200-mW. At a 1-to-2 kbit/s data rate, these low-power systems usually have an effective range of 150 to 300 feet indoors and roughly 800 feet outdoors. IR systems generally have range of between 30 and 50 feet. This means that any long-haul data transport must be done by accessing the wired portion of the LAN through some sort of access point. Rather than being a disadvantage, the limited range makes it possible to create small microcells within a LAN to support more users, or operate several independent networks in a limited area.

Within the U.S., there are currently three bands, known as the ISM (industrial, scientific, and medical) bands, allocated for unlicensed wireless network activities. Their frequencies, which are between 902 and 928 MHz, 2400 and 2478.5 MHz, and 5725 through 5850 MHz, are used for many applications as well as wireless LANs. Depending upon frequency and location, a LAN system may have to share the airwaves with other LANs or other applications.

Each frequency range has its own set of advantages and problems. The 900-MHz band is currently inhabited by advanced cordless telephones, security systems, and baby monitors, and PCSs are expected to join in the future. The 2400-MHz band offers reasonably good propagation characteristics and has the advantage of nearly global designation as a wireless communication spectrum. Unfortunately, the other applications already operating at 2.4 GHz may be noisy neighbors. Because a 2.4-GHz network sits within a popular portion of the ISM band, it can expect to share its frequency slot with an odd assortment of users, including diathermy machines, microwave ovens, and licensed high-power users (police, railroad workers, and scientific telemetry transmitters). Less favorable propagation characteristics and high component costs have slowed development of systems operating in the 5.7-GHz band.

Though worse at 5.7 GHz, RF transmissions at all of these frequencies are subject to Rayleigh

STANDARDS WARS IN THE WIRELESS WORLD

Since they were introduced in the U.S. 12 years ago, the growth of cellular telephones has far outpaced the forecasts of the wisest industry pundits. The current analog cellular-telephone system, the Advanced Mobile Phone System or AMPS, is fast approaching capacity in many markets. Time-division multiple-access (TDMA) and code-division multiple-access (CDMA) have emerged as the two competing digital standards offering greater bandwidth and improved transmission quality.

The FCC has allocated a 50-MHz (824 to 894 MHz) carrier bandwidth for the cellular network, within which AMPS uses frequency-division multiplexing to create 30-kHz channels, each supporting a single call. To promote competition, the FCC allows the 50 MHz to be split between two carriers for each cell. This leaves each carrier with 25 MHz that's divided into 12.5 MHz for transmit and receive bands. The bottom line is about 54 channels are available for cellular traffic.

TDMA converts analog speech to digital signals using a fixed-rate vocoder. The signal is transmitted on a 30-kHz bandwidth like AMPS, but 3 callers share multiplexed time slots on one channel).

CDMA uses a spread-spectrum technique to spread the digital signal over 1.25 MHz. Speech is digitized using a variable-rate vocoder, and each voice is assigned a unique code. The signal is then modulated across the entire 1.25-MHz band. The intended receiver demodulates the signal using its appropriate code. The vocoder uses Qualcomm's code-excited linear-predictive (QCELP) speech-encoding algorithm to transmit speech at minimum data rates. Qualcomm claims an average data rate of under 4 kbits/s for QCELP, which results in higher capacity, lower transmitted power, and lower interference.

CDMA proponents claim a 20-fold increase in capacity over AMPS and a 7-fold increase over TDMA. Proponents of TDMA counter that this can only be achieved on paper. They're working on extended TDMA (ETDMA), which uses a half-rate vocoder to increase the capacity to 15 times the AMPS system (TDMA currently uses vector-sum-excited linear-predictive (VSELP) coding to reduce the 64 kbits of data required for one second of speech to an 8-kbit/s data rate). The CDMA camp concedes that capacity increases of 10 to 15 times the analog approach are probably more realistic than 20 times, but they argue that ETDMA won't live up to advertised claims either.

There are other important issues involving soft handoff of calls as the user passes from one cell area to another, such as voice quality, power consumption, and the range of each cell (CDMA cells reportedly have greater range, which translates into installing fewer million-dollar cells). Both CDMA and TDMA have been approved by the Telecommunications Industry Association as IS-95 and IS-94 standards, respectively. TDMA has about a one-year jump on CDMA in implementation, with early sites being installed in 1994. CDMA will start installing systems in 1995. It's anybody's guess as to which standard will prevail.

Many areas are going to an enhanced version of the analog system called NAMPS, developed by Motorola as a bridge, until a digital systems come on line. NAMPS increases capacity about 3X over AMPS. Added to the mix is the scattering and reflected signals, which can cause signal strength to vary by a factor or 1000 within the space of a meter. Most of these physical effects are dealt with at the physical layer before the protocol takes over. But some things like signal strength must be monitored carefully at a higher level to facilitate such functions as selecting an access point to talk to, moving between access points, and controlling output power or receiver gain.

It's in these challenging environments that the network must support data transfers and extract information with a low error rate (1 part in 10^{-5} is considered a typical minimum). Because the bit rate for an RF link is typically much lower than a wired network (250 kbits/s to 2 Mbits/s), any error-control techniques must be efficient. Otherwise, they will significantly impact overall system throughput.

Traditional traffic-management techniques like collision detection are inefficient for wireless LANs. Since it's nearly impossible to detect a collision in a wireless environment until after transmission, some sort of collision avoidance scheme should be employed.

WHAT TYPE OF CONTROL?

When implementing collision avoidance, one must choose whether to impose centralized control on all network nodes via a point-control function scheme or give each node independent collision-avoidance capability and implementing a distributed-control function.

A centralized point-control function scheme prevents collisions by taking rigid control of all nodes and allowing only one unit at a time to talk *(Fig. 1)*. This method offers the advantages of low transmission overhead and can easily support time-bounded data, such as voice and video. With a strict point-control-function architecture, ad hoc or peer-to-peer networking outside direct network control only can be done if at least one node provides the coordinating functions of the network's access point. Designers must either equip each node with extra hardware and software required for point control, or limit system flexibility.

Distributed-control structures, which offer the advantage of flexible peer-to-peer operation, support temporary, secure, ad hoc mini-networks without relying on the LAN. As a result, people can work more naturally, exchanging data at meetings and within workgroups regardless of location. Another consideration is how to guarantee access to the network for all units in the area. Without the central control of a point-control method, each distributed-control node must possess a set of "manners," which prevents any single unit from hogging a disproportionate share of the LAN's time. Critics of distributed control contend that providing these features requires increased transmission overhead, thus reducing efficiency. Fortunately, the lessons learned from earlier protocols have yielded designs that keep the extra overhead to a minimum.

At the MAC level, other dilemmas arise that are unique to the wireless environment. One classic example is referred to as the "hidden node" problem. Because portable systems may be distributed at random throughout the reception area of an access point, two nodes may not be able to hear each other when both try to communicate with the LAN, causing both transmissions to be lost. In addition, the mobility of the data sets dictates that some hand-off procedure must be devised to allow a node to change access points as it moves through the building or campus.

There's still much controversy about which frequency-control scheme is best for wireless LANs. FCC rules for the ISM (1.9 to 2.4 GHz) band re-

fact that CDMA and TDMA also are going head to head for PCSs and wireless local loops.

In the private-network arena, wireless LANs offer several advantages over traditional hardwired LANs. Most notably, they're flexible and give users mobility while maintaining a link to the LAN. The IEEE has tried to keep WLANs from encountering the confusion over standards found in the cellular world by developing a unified MAC protocol that's consistent with the OSI protocol stack. The IEEE 802.11 Committee has spent the last two years trying to agree on a standard that will satisfy the broad range of applications and proprietary interests of the companies sitting on the committee.

Up until this past November, the committee was divided between several MAC-layer proposals. In fact, at one point, it appeared that the winning vote would be "not ready to decide." National Semiconductor felt that this was unacceptable and withdrew their proposal from consideration to back the proposal being put forward by NCR, Xircom, and Symbol Technology. It's expected that the new standard will be formalized around July 1995 but companies will begin shipping products conforming to the proposed standard later this year.

The proposed 802.11 standard defines the MAC layer and at least one physical layer for a wireless LAN. A wireless LAN in this context is non-tarriffed transmissions confined to a local area. Cellular and WAN transmissions aren't covered in this standard.

The proposed standard emerged by taking concepts from IBM's and Xircom's proposals and combining the two in a Super Frame that allows the deterministic and non-deterministic portions of the protocol to reside in separate parts of the frame. The initial proposal defines a physical layer for 1-to-2-Mbit/s rates and the next generation of technology will support speeds of up to 20 Mbits/s. Another subcommittee is working on an infrared physical layer. Voting to formalize these layers should be complete by late 1995.

Contributed by James Scheussler, staff applications engineer for the Innovative Product Division at National Semiconductor, Santa Clara, California.

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	14SOIC	16SOIC	28PLCC	44PLCC	68PLCC	84PLCC	100PQFP	100PQFP	144PQFP	144PQFP	160PQFP
		14SOIC	20SOIC	28PLCC	44PLCC	68PLCC	84PLCC	84PLCC	100PQFP	100PQFP	144PQFP
			16SOIC	20SOIC	28PLCC	44PLCC	68PLCC	68PLCC	84PLCC	84PLCC	100PQFP
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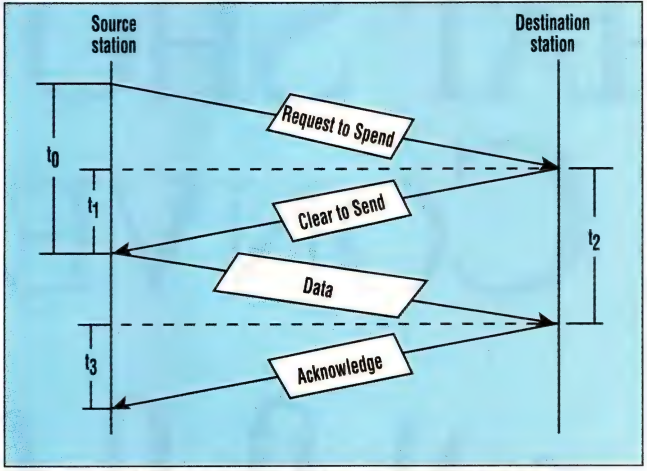
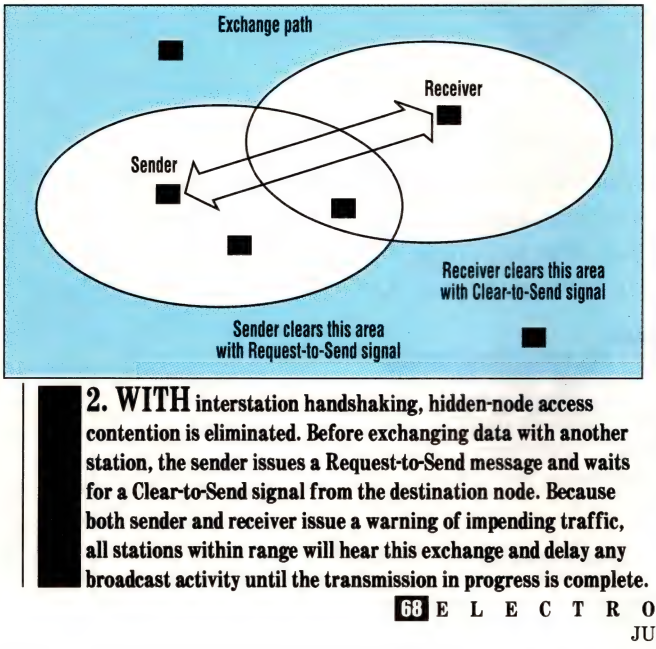
quire that users employ some form of spread-spectrum technology. Most experts agree that even in bands where it's not required, spread-spectrum technology is an effective way to communicate in a noisy environment. Support is divided however, between direct-sequence and frequency-hopping spread-spectrum techniques used to overcome background noise and manage spectrum use. Rather than wait years for resolution or impose a potentially incorrect decision, the IEEE 802 Committee's working group has established standards that support both schemes. In theory, the market will act as the final arbiter.



3. AN ASYNCHRONOUS TRANSACTION is framed by the Request to Send, Clear to Send, and Acknowledge exchange frames. Transmissions between nodes employ Request-to-Send and Clear-to-Send signaling to alert the receiver, clear the channel, and enable the transmitter. The Acknowledge signal issued by the receiver at the end of the transmission verifies receipt of the data. To reduce overhead, short messages (typically less than 100 bytes) may forgo the Request-to-Send signal but still require an Acknowledge signal to complete the transaction.

All of these concerns have gone into the development of the IEEE 802.11 standard. Like its other, more well-established cousins, such as the 802.3 standard (better known as Ethernet), this protocol allows multiple workstations to transport data on one frequency band. The committee members to applied the lessons learned from development of previous protocols to the unique challenges of the WLAN environment. Although work on the specification is still ongoing, it well enough defined to make a closer look very worthwhile.


Exchange path
Receiver
Sender
Receiver clears this area with Clear-to-Send signal
Sender clears this area with Request-to-Send signal

2. WITH interstation handshaking, hidden-node access contention is eliminated. Before exchanging data with another station, the sender issues a Request-to-Send message and waits for a Clear-to-Send signal from the destination node. Because both sender and receiver issue a warning of impending traffic, all stations within range will hear this exchange and delay any broadcast activity until the transmission in progress is complete.

To really understand 802.11, it's best to look at the network from the perspective of a handheld, mobile computer. Upon waking up, the first order of business is to turn on your receiver and listen to traffic. Scanning quickly, you notice clear, strong signals on one of your assigned channels. Rather than jump in immediately, you remember to follow the rules of 802.11 and wait for a time when nobody is talking. You then issue a short message addressed to the access point that contains your ID number, and possibly an encrypted password along with a request for permission to "associate" with the network. Your request is passed on to the network server, which controls access and security. Once your identity is validated and appropriate encryption is established, the network returns an association response message to you. Welcome aboard the net.

Once logged on, life inside the network is fairly simple. Much of your time is spent listening to the traffic whizzing by. Since any messages can be flagged by looking for your address in the short message header, you can spend much of your time taking catnaps in a power-saving mode. When you have something to say, you wait until nobody is talking and issue a short request-to-send (RTS) message, containing the address of the targeted access point or node *(Fig. 2)*. The RTS message also contains the network allocation vector (NAV), a delay time based on the size of the message you want to send. Once ready, the destination station will issue you a clear-to-send (CTS) message and echo the NAV (transmission duration).

This simple handshaking between nodes serves to get the destination ready to receive a message; the broadcast NAV tells all of the other nodes on the network how long you intend to be talking. Because the other nodes are just as "polite" as you are, they will delay transmitting for the period you specified, plus an extra random back-off interval. Once you transmit your message, you then listen for an Acknowledge signal from the target station *(Fig. 3)*. If there's no Acknowledge signal or if the Acknowledge signal's status word indicates that there were errors, you must attempt to retransmit at the next possible opportunity.

Note that the "hidden node" problem is solved because both the transmitter and receiver broadcast the NAV, so any other station within earshot will know that there's a conversation going on. In the rare cases that a hidden node barges in before the RTS/CTS handshake is complete, the protocol will force all parties to back off and try again.

Sometimes stations will want to transmit very short messages (less than 100 bytes) that aren't much larger than the overhead required to transmit them. These short messages transmit network-manage-

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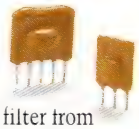

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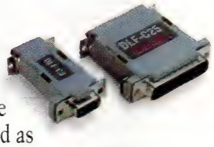

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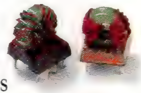

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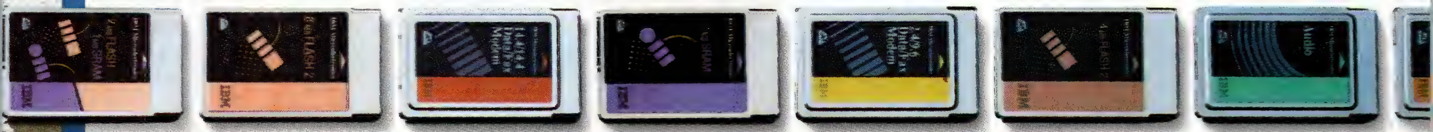

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ment information as well traffic-indication alerts, which are broadcast to stations, alerting them to prepare for incoming traffic. For the sake of network efficiency, stations may simply send short packets instead of the RTS signal and forgo the CTS handshake. An Acknowledge signal, however, is still required to complete the transaction.

DUAL MODE IS FLEXIBLE

Perhaps the most unique feature of the 802.11 protocol is its ability to function well in point-control-function and distributed-control-function environments. This means that any compliant node device can operate as part of a large, centrally-controlled LAN or form an ad hoc workgroup in a hotel lobby or at a poolside table.

The protocol developed by the 802.11 working committee is a hybrid system that combines most of the strengths of the point-control-function and distributed-control-function access schemes. Rather than force wireless devices to run two separate protocols, this blended system uses distributed control as its foundation and then builds a central-control structure on top of it.

The basis for the 802.11 MAC is a distributed coordination function designed to provide equal access to the wireless media for all stations. The protocol recognizes that the highest probability for collision immediately follows a busy period (because frames could be queued during that busy time). Distributed-control operation uses the RTS/CTS handshake signal to control traffic and the NAV embedded in each exchange to moderate access contention between stations. Adding a random backoff delay to the NAV assures that eventually every station will be the first one to request a turn.

As part of the management scheme, each station possesses its own unique 48-bit IEEE device code. When associated with a workgroup, the station carries a table of the other group member's ID codes. Each node also shares a common association password, used to protect workgroup security. Under this structure, ad hoc networks can be established and disbanded easily.

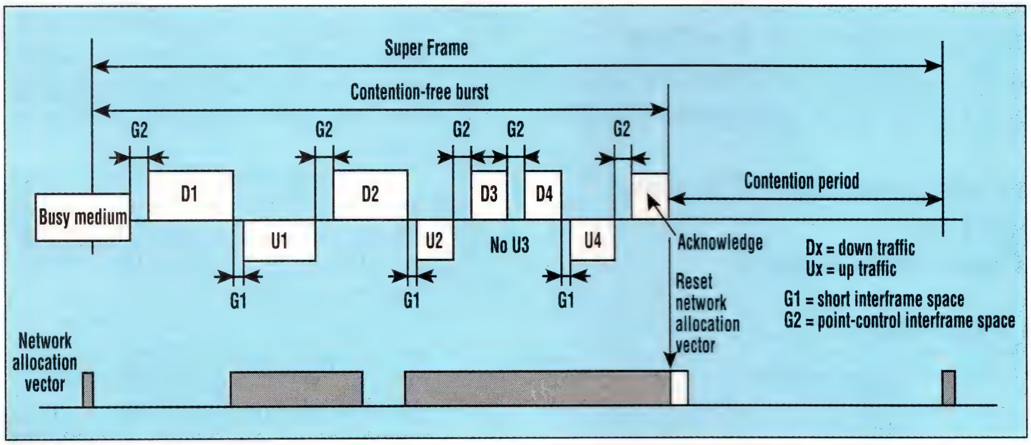
When working in a LAN environment, the point-control function can be established simply by exploiting the fact that all stations must wait for a minimum fixed period before trying to request media access. This period is referred to as the interframe space, or IFS *(shown as* G_2 *in Fig. 4)*. Under the 802.11 protocol, a point-control-function station can take control of a group simply by transmitting before any other station's NAV times out. Once in control, it keeps the channel "busy" and off-limits to any "normal" stations.

Having acquired a channel, the point-control function polls each active node in the network, using a list it maintains. During this polling period, the point-control function can transmit data to a station as well as receive it. This time slot, in which all active stations are accessed sequentially, is known as the contention-free period because nodes aren't allowed to contend for the media on their own.

After the contention-free period, the "contention period" time slot opens up. Here, any station can request access to the point-control function by using the distributed-control-function protocol. The contention-period length is set by the access point of the point-control function but has a minimum length determined by the time required to transmit a maximum-size frame (about 500 bytes). Nodes that are silent for too long may be dropped off the active roster to save overhead. Inactive nodes still associated with the network may regain active status by issuing a request during the contention period.

The 802.11 MAC provides both types of access during each Super Frame (non-contention plus contention periods) to allow the highest possible operating efficiency under varying network conditions. In light traffic, the distributed-control-function-based contention period offers quick access and lower overhead. As network loading increases (usually around 6 or more nodes), distributed control begins to use more of its time resolving access contention and less time moving data. The contention-free period's efficiency is much less affected by heavy network traffic.

Since all stations are driven by the point-control-function node controller, adjustments to the time periods within the Super Frame can be made easily. With a well-designed traffic-management algorithm, a point-control-function node could ad-



4. A SUPER frame structure defines transactions under a point-control function. The Super Frame consists of 2 major time periods, the contention-free period and the contention period. During the contention-free period, the point-control function access point broadcasts a message within the point-control interframe space (G_2) before any station's backoff period expires and gains control over the channel. The point-control function then polls each active station sequentially, uploading or downloading data as required. A contention period follows that allows stations to interact freely in a distributed-control mode. At the end of the contention period, the point-control-function node asserts control again and begins a new Super Frame.

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just contention-period duration, according to system loading, for the highest network efficiency. Equally important, the independent nature of the remote nodes permits upgrades to point-control-function access points with no need for the modification of node-station hardware or software.

FREEDOM TO ROAM

The ability to maintain contact with mobile nodes as they "roam" between access points is an important MAC function, and is currently being developed. Though all of the details aren't firm yet, the general structure is in place. Unlike cellular telephones, wireless LANs will allow their mobile nodes to hand themselves off between access points at will, rather than under the network's control. The station will keep track of all access points within its range and autonomously select the one with the best signal.

The 802.11 protocol is designed with features that support multimedia applications. The contention-free period within each Super Frame can handle transmission of time-bounded data, such as sound or compressed video. Recently, however, a proposal was made to modify the protocol so that isochronous data also could be handled during the contention period. Other features of the protocol still being defined include the sequences that will permit a station to quickly reassociate with a network after a brief interruption, without a complete and time-consuming trip through the full association procedure.

An anticipated initial release date in early 1995 has the 802.11 Committee scrambling to address many other difficult technical issues. Nevertheless, a number of the major architectural questions have been resolved, and it appears that a network protocol which can provide a sturdy framework for the wireless infrastructure of the future is near fruition.☐

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-1 dBm PSAT
7.5 mA Icc

UPC2747
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100 MHz to 1800 MHz
12 dB Gain
3.3 dB NF, 5 mA Icc

UPC2746
High Gain Amplifier
DC to 1500 MHz
19 dB Gain
0 dBm PSAT
7.5 mA Icc

UPC2748
High Gain Low Noise Amplifier
200 MHz to 1500 MHz
19 dB Gain
2.8 dB NF
6 mA Icc

UPB1502
Frequency Divider
0.5 to 2.2 GHz
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6 mA Icc

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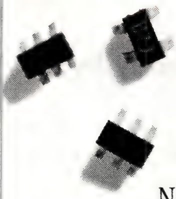

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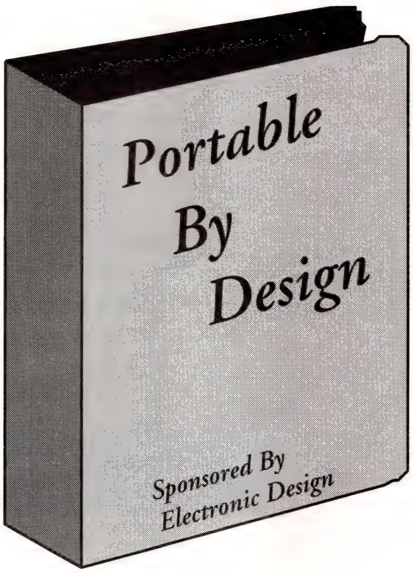

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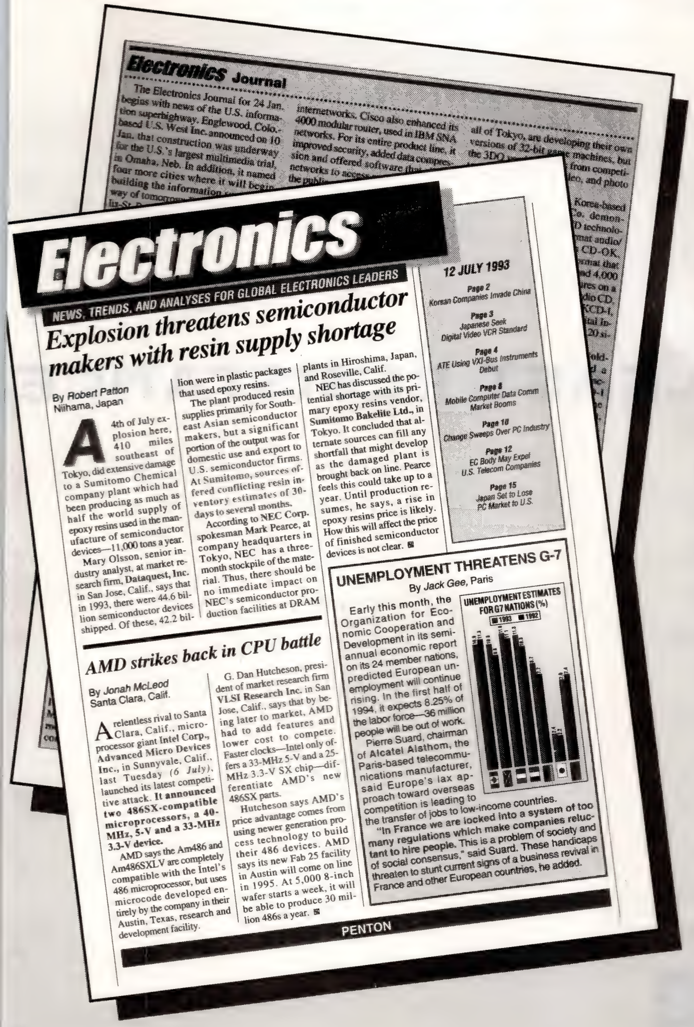

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Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

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Japan Set to Lose PC Market to U.S.

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manepoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to NEC Corp. spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ■

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant Intel Corp., **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ■

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of Alcatel Alsthom, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

UNEMPLOYMENT ESTIMATES FOR G7 NATIONS (%)

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ONE CHIP SQUEEZES IN A 68000 CPU CORE, A 24-BIT DSP ENGINE, A PCMCIA CONTROLLER, AND MULTIPLE HIGH-SPEED SERIAL CHANNELS.

NO-COMPROMISE CONTROLLER COMBINES DSP, DATA COMM

DAVE BURSKY

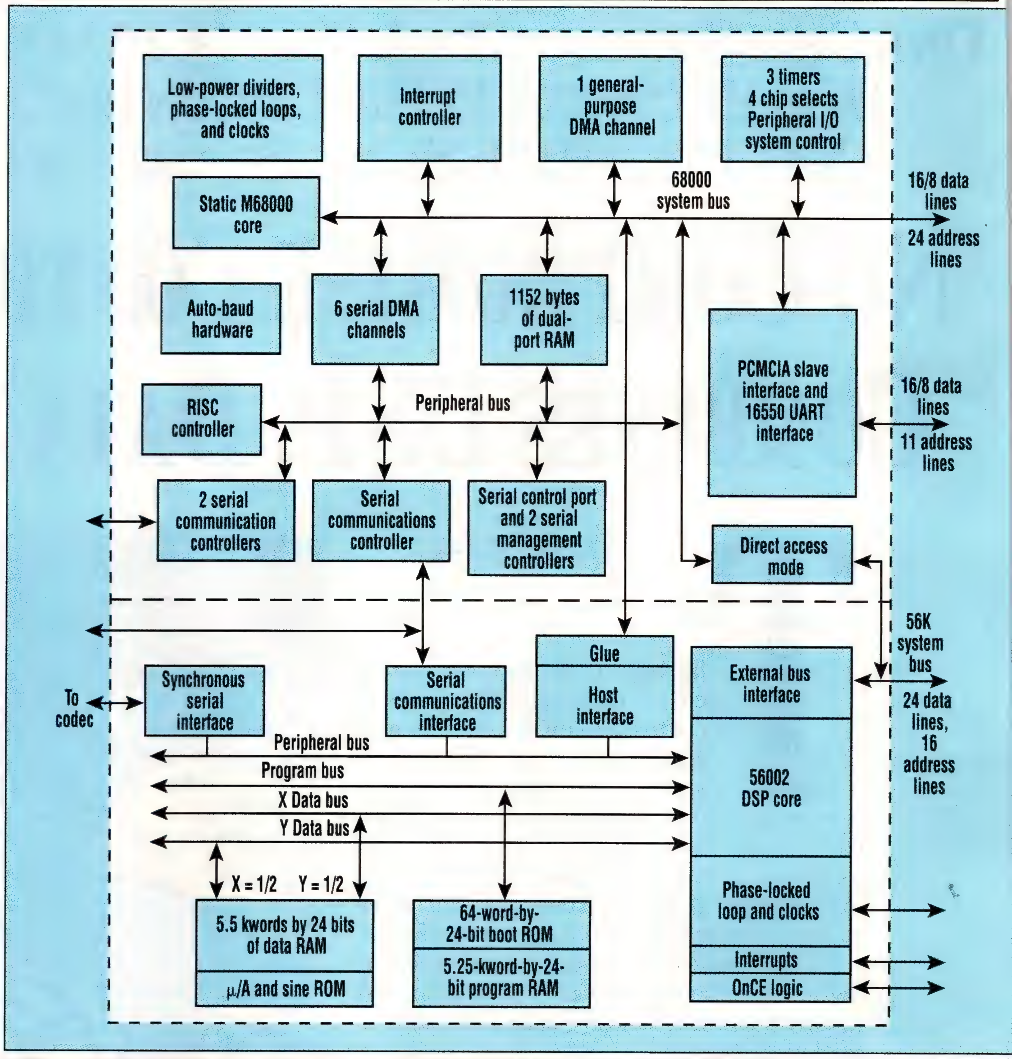
The one tenet designers must consistently follow is simple in context but difficult to achieve: Have systems do more in less space. Conventional microprocessors and even the latest control-oriented RISC processors don't have enough on-chip resources to deliver the necessary processing throughput. Multichip solutions can solve some of the problems, but poor interprocessor communications, limited board space, or higher-than-desired power consumption will thwart such solutions for many of their intended applications.

Some microcontroller manufacturers have come up partial solutions, for instance by adding sub-processors such as 8- or 16-bit DSP blocks, special function blocks such as communications subprocessors, or arrays of timers. But these answers deliver limited performance gains because each block often strikes a compromise between performance and cost.

Designers at Motorola have now come up with a better solution in the MC68356 controller. It provides the first no-compromise approach by combining multiple high-performance processors on one chip. The chip incorporates a 32-bit 68000-family-compatible core to coordinate all operations, a full 24-bit high-performance digital signal processor, a RISC-based multichannel communications processor, abundant memory resources, and various system support logic that includes a full PCMCIA interface *(Fig. 1)*.

Furthermore, the chip's resources were optimized for low-power applications, thus suiting it for many battery-powered data- and voice-communications systems. The 68356 combines the features of both Motorola's 68302 integrated multiprotocol processor and the company's 56002 24-bit digital signal processor. And, with the additional system resources it provides, the chip can solve problems that even multichip solutions are unable to handle.

With so many on-chip resources, Motorola's designers had to resort to some innovative packaging to provide many I/O, address, and data lines without using a large package. As a result of their innovative approach, the 68356 is the first microcontroller to use a 357-contact ball-grid-array package. The package occupies only about 1 square inch of pc-board space and has a height of less than 50 mils, suiting it well for small-format products like PCMCIA cards and disk drives. In addition, the solder bumps that make contact to the pc board eliminate the manufacturing hazards of bent leads on high-pin-count packages.


Low-power dividers, phase-locked loops, and clocks
Interrupt controller
1 general-purpose DMA channel
3 timers 4 chip selects Peripheral I/O system control
Static M68000 core
68000 system bus
16/8 data lines
24 address lines
Auto-baud hardware
6 serial DMA channels
1152 bytes of dual-port RAM
PCMCIA slave interface and 16550 UART interface
16/8 data lines
11 address lines
RISC controller
Peripheral bus
2 serial communication controllers
Serial communications controller
Serial control port and 2 serial management controllers
Direct access mode
56K system bus
Glue
Host interface
External bus interface
24 data lines, 16 address lines
To codec
Synchronous serial interface
Serial communications interface
Peripheral bus
Program bus
X Data bus
Y Data bus
56002 DSP core
X = 1/2
Y = 1/2
5.5 kwords by 24 bits of data RAM
µ/A and sine ROM
64-word-by-24-bit boot ROM
5.25-kword-by-24-bit program RAM
Phase-locked loop and clocks
Interrupts
OnCE logic

1. THE BEST OF SEVERAL PROCESSORS ARE COMBINED in the 68356 designed by Motorola. The chip incorporates a 32-bit 68000-based static CPU core. In addition, it holds many other circuits including a 24-bit high-performance digital signal processor; a PCMCIA slave interface; a RISC-based, high-performance, multichannel, serial data-communications controller; and abundant system interface and memory resources.

Besides handling general-purpose embedded control applications, the 68356 eases the development of intelligent high-performance modems, cellular telephones, industrial control systems, and other systems that require the confluence of DSP and advanced communications control. Part of that flexibility is due to the trio of communication interfaces included on the chip—a host interface that can tie into a central processor, an asynchronous serial communication interface (SCI), and a synchronous serial interface (SSI). The SCI serves as an RS-232 type of interface that can communicate with such devices as modems, microcontrollers, and terminals, while the SSI provides a flexible synchronous link to high-speed devices like codecs and analog-to-digital converters.

In addition to the 68356 user-programmable version, designers at Motorola preprogrammed one version, the 68356M, to serve as a data pump for data-communications applications (e.g., modems). Due to the on-chip resources, the chip can serve well in multifunction applications that, for example, would combine the modem and a network interface. The preprogrammed functionality lets the chip serve as either a V.22bis, V.32, or V.32bis modem, as well as comply with the latest V.34 (V.Fast) standard.

The heart of the 68356 consists of two familiar processing units—the 68000 CPU core, and the 56000 DSP core. Supporting the DSP core are 5.25 kwords (24 bits/word) of program RAM and 5.5 kwords (24 bits/word) of data RAM. Although both cores can operate from the same external clock source (either a crystal or an oscillator), they also can run asynchronously, each with their own clock source. The on-chip clock oscillators use external crystals ranging from 32 kHz to 6 MHz; above 6 MHz, an external oscillator(s) must be used to supply the master clock signals.

The 68000 core processor will initially operate from a 25-MHz external clock when powered by a 5-V supply (increasing to 33 MHz in 1995), and back off to 20 MHz when the supply is set at 3.3 V. That core was redesigned for fully-static operation, making it possible to slow or stop the clock to minimize power drain when idling.

The DSP engine can run from either the same clock or a separate clock source, therefore it can operate at internal speeds of up to 60 MHz. That's because an on-chip phase-locked loop bumps up a 32-kHz-to-6-MHz external clock to the desired clock frequency, or multiplies the

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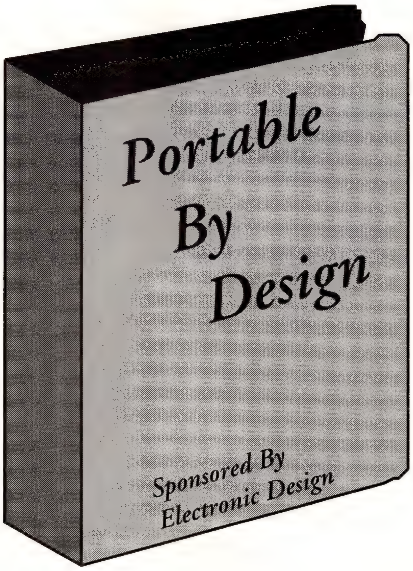

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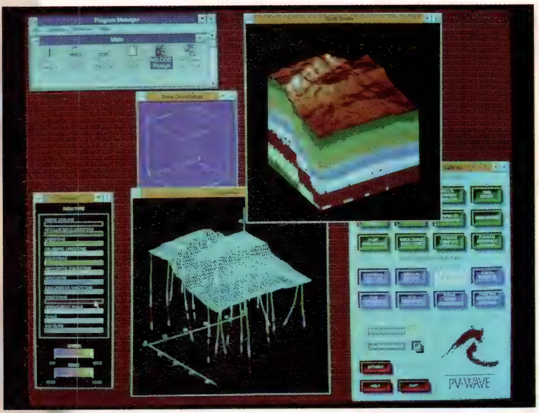

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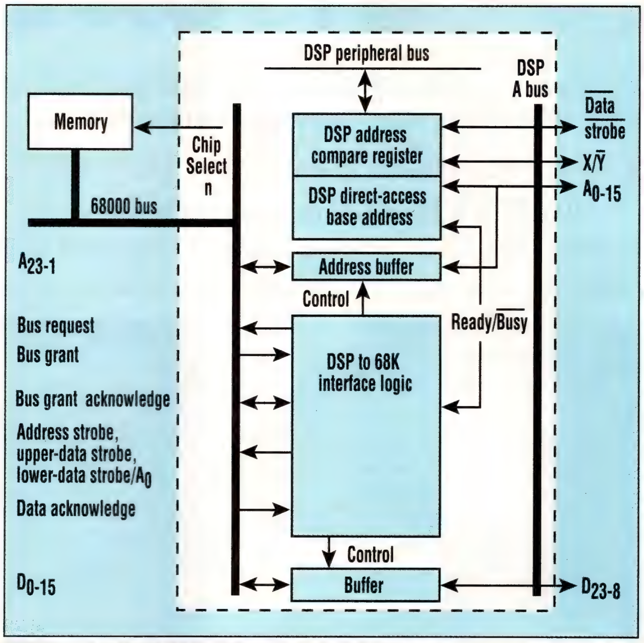
clock signal from an external oscillator.

When running at full speed, the chip consumes about 1 W from a 5-V supply and about 300 mW from a 3.3-V supply. Standby and power-down modes drop the power drain to just a few milliwatts.

The DSP engine contains three separate and concurrent execution units—the arithmetic and logic unit, a program control unit, and an address-generation unit. In addition to the chip that contains both program and data RAMs, versions with program and data ROMs or some mix of the ROM and RAM can be created to suit various cost points. Typically, more ROM can be included on the chip (10 times the amount of RAM storage) if large programs are required, or if large, fixed-data tables are used.



2. COUPLING THE DSP ENGINE to the 68000 core requires some interface logic that helps arbitrate the bus accesses. Address comparators first check the address range of the access request. If there's a match, the arbitration request proceeds using the Bus Request, Bus Grant, Bus Grant Acknowledge, and other control signals.

The digital signal processor's extended Harvard architecture provides three separate buses to connect the execution units to internal memories. Thus, the engine can obtain two data words and an instruction in a single instruction cycle. There's lots of addressing flexibility due to the DSP engine's three types of address arithmetic—linear, modulo, and reverse carry. In addition, the engine includes hardware Do loops that help with repetitive operations, and a fast-interrupt function that lets the processor handle the interrupt and return to earlier tasks quickly.

To facilitate the interprocessor communications on the chip, Motorola's designers added a special interface logic block that ties the 56000's core DSP A bus to the 68000 CPU *(Fig. 2)*. Because the DSP-to-68000 interface allows the DSP core and software to access data in the 68000's memories, system cost is reduced since both cores use a common memory.

However, that access must be synchronized and will add some software overhead to poll the internal Ready/Busy signal bit, compared with other DSP accesses. Thus, the DSP core has several options for storing data—use either the large internal DSP memories, external memory connected to the DSP buses, or external memory connected to the 68000 buses.

Furthermore, the SCI channel is physically connected to one of the controller's serial communication channels (SCC1), providing a direct serial link through which data can be passed at high transfer rates. In a modem application, such a scheme would permit the DSP engine to apply modulation and filtering to the incoming signal. Then the data is streamed to the communications engine, which would then perform the formatting, compression/decompression, or some other task.

Users can select which memory is employed based on performance and cost trade-offs. Internal memories permit the fastest operation, but have limited capacity. External static memory tied to the DSP port is slightly slower than on-chip memory and adds considerably to the subsystem cost, but still permits fast accesses. Finally, the slower external memory tied to the 68000 expansion buses offers the lowest performance, but also has the lowest-cost/highest-density option if DRAMs are used.

When the DSP block initiates a Data-Write operation to its external bus, the bus interface logic compares the $A_{15\text{-}12}$ address lines to the programmable value. If matched, the logic sets the Busy bit, samples the data and address bits, and arbitrates for the 68000 bus. Once bus access is granted, a standard 68000 write cycle occurs. The high address bits and function-code (FC) bits are taken from the DSP base-address register and the low address bits are taken from the sampled DSP address lines. When the cycle is terminated with the Data-Acknowledge signal, the 68000 bus is released and the Busy bit is reset to the Ready status. A similar sequence occurs for a read cycle. Furthermore, these processes have priorities over the PCMCIA direct-access mechanism and are unaffected by the external Bus-Clear signal.

One key feature that leverages the low power and communications capability of the 68356 DSP controller is a PCMCIA slave interface *(Fig. 3)*. By using such an interface, the 68356 can form the heart of intelligent I/O cards that plug into host systems with PCMCIA slots. Functions possible in the PCMCIA format include modems, network interfaces (including the Integrated Services Digital Network), and multimedia sound cards.

The interface incorporates a full set of signals and registers as specified by the 2.1 release of the PCMCIA standard. Five configuration registers are supported as well as programmable address spaces and an unlimited number of attribute memory bytes. The controller also performs transfers from the PCMCIA attribute and common-memory space cycles into the 68000 bus with three base address registers. Transfers using a cycle-stealing scheme or burst-transfer arbitra-

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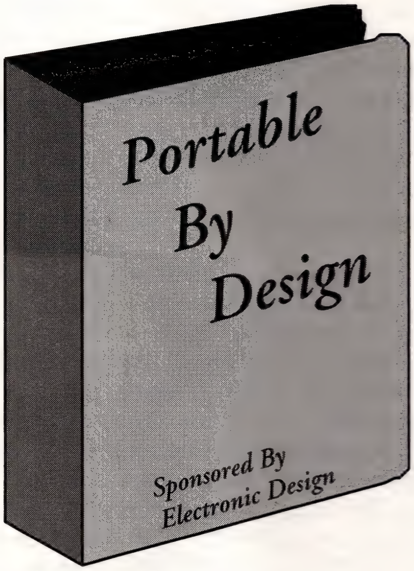

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tion also can be done over the PCMCIA interface.

When the 68356 DSP controller is reset, the PCMCIA controller assumes the default "memory only" card configuration, with the Ready/Busy signal going low to indicate the Busy condition. The 68000 core then initializes the card-information-structure (CIS) base-address register with the high address of the external CIS memory address. The CIS memory can be located in external RAM or ROM, while the five configuration registers are positioned on the PCMCIA attribute address space ($A_{25} = 1$). The CIS's configuration table TPCC_RADR (tuple card configuration register address) should have the base address of these registers. If so, the 68000 core can signal that the card is ready by bringing the Read/Busy signal high.

The host reads the first value of the CIS from attribute memory by performing an attribute-space read cycle to address 0. The PCMCIA controller detects the cycle, asserts the Wait signal on the PCMCIA lines, and arbitrates for the 68000 bus. When the bus is granted, the PCMCIA interface will then generate the cycle on the 68000 bus. The high address bits and function code are taken from the CIS base-address register. Low address bits come from the PCMCIA address lines.

When the cycle is terminated with the Data Acknowledge signal, the 68000 bus is released, data is transferred to the PCMCIA data lines, and the Wait signal is negated. The host also can initialize the CIS registers without using the 68000 bus: When address A_{25} is high on an attribute-space cycle, the PCMCIA controller asynchronously accesses the configuration registers. Or, the 68000 core can access those registers, and read from or write to them just as it can to any register in the 68356 DSP controller's address space.

Furthermore, the PCMCIA controller can generate an interrupt to the 68000 core when one of the registers is written by the host. Once the interface is configured for PCMCIA I/O transfers, I/O data transfers are used to read and write the 16550-compatible registers that set up the emulation of a 16550 universal asynchronous receiver/transmitter (UART). The host transfers data to and from the card by writing and reading to and from the 16550 FIFO buffer. I/O accesses are connected directly to the 16550 emulation logic without using the 68000 bus.

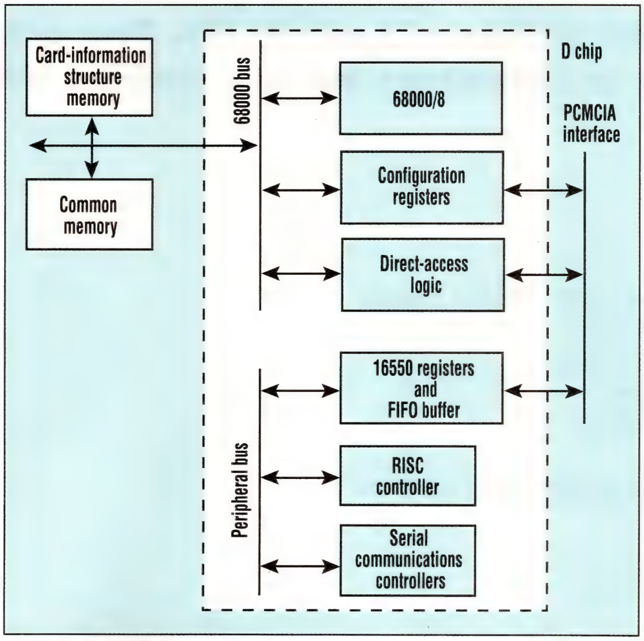
Another scheme that transfers data and commands between the host and card—the direct-access mechanism—also is supported by the chip. In this mode, PCMCIA common-memory space accesses are mapped into the 68000 bus. Such a scheme is good for fast data transfers between the card and the host when software compatibility with IBM-compatible PCs isn't important.

The communications block on the chip contains three serial communication channels controlled by their own dedicated RISC processor. As a result, the serial ports can operate independently of the 68000 host, transferring information, dealing with the serial channel interrupts, and performing the protocol-processing functions, all independent of the 68000 CPU. That leaves the 68000 core free to handle higher-level control tasks.

The 68356 uses an enhanced version of the communications block present on Motorola's 68302 integrated multiprotocol communications processor. The three serial channels on the 68356's communications subprocessor can operate independent of each other. Each channel can transfer data using a different protocol, allowing the controller to serve as a "bridge" between two or three systems. Each channel also includes a pair of on-chip DMA controllers, one for receiving and the other for transmitting. Consequently, the subprocessor can transfer data without requiring any attention from the 68000 host.

Protocols supported by the subprocessor include high-level data-link control/asynchronous data-link control (HDLC/SDLC), asynchronous UART, and BiSync. Moreover, a "transparent" mode permits users to disable selective elements of the hardware-based protocols and substitute customized software routines. That allows the chip to readily adapt to non-standard communications applications. In addition to the three high-level serial channels, which are targeted at network interfaces, the 68356 includes a simple serial communications port. Using this port, the chip can readily communicate with other system components, such as voice coder/decoders, real-time clocks, 8-bit microcontrollers, as well as other digital-signal processors.

The 68356 DSP controller chip provides a collection of resources to help control and coordinate system activity. Its system integration block includes an 1152-



3. A FULL PCMCIA slave interface is included on the 68356. With such an interface, the chip can be used in PCMCIA cards. It also provides a fully-compatible interface to the 2.1 version of the PCMCIA standard. The configuration registers and direct-access logic make it possible for the chip to operate either in the standard PCMCIA software-compatible modes, or in a unique mode that enables the interface to minimize system overheads and perform rapid data transfers over the PCMCIA interface.

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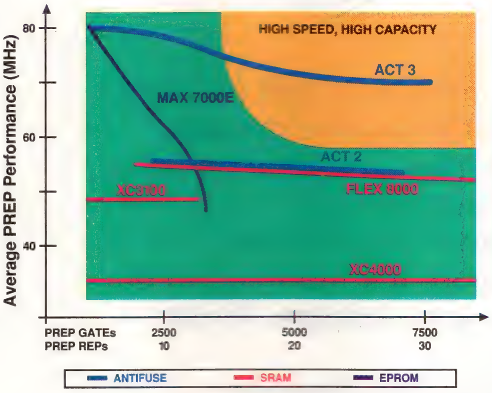

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byte dual-port RAM that provides two system support functions. Part of the memory serves as a memory-mapped register bank through which the central processor communicates with the serial channels and other system functions. The other part (576 bytes) serves as on-chip data buffers or general-purpose memory. Other logic in the system-integration block includes a DMA controller, two general-purpose counter-timers, a clock generator, an interrupt controller, parallel I/O ports, and chip-select and wait-state logic.

The complexity of the 68356 may cause some concern on how such a device will be tested or emulated during system debugging and diagnostics. That's why the company-developed on-chip emulation (OnCE) capability was integrated into the logic, establishing essential debugging functions in the processor hardware itself.

Both the 68000 processor and the 56000 DSPs have extensive libraries of software and a wide range of development tools already available from Motorola and many other sources. Virtually all of those tools can be employed to develop the software for the 68356.

On top of that, Motorola created the 68356 application development system, which consists of a development board containing the processor and an RS-232 port that can connect to a dumb terminal, a PC, or a Sun workstation. The board includes the OnCE background debugger and a command converter for on-chip emulation of the 56002. Board-resident debuggers are available for both the controller as well as the DSP engines.☐

PRICE AND AVAILABILITY

The MC68356 DSP controller comes in a 357-lead ball-grid array package and sells for $64.95 each in lots of 10,000. Samples are immediately available.

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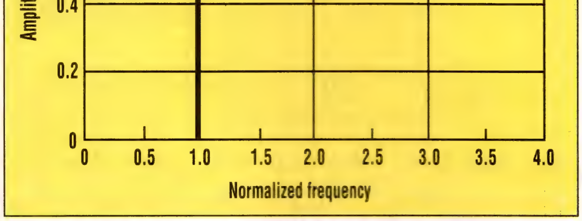
Communications channels need to carry as much information (or data bits) within their assigned bandwidths as is physically practical. This practicality is forever challenging the communications engineer, who continually strives to squeeze more data into less bandwidth with clever coding schemes. For instance, digital-coding schemes like pulse-amplitude modulation (PAM) have evolved from a single threshold level between 1 and 0 (typically 2.5 V) into systems with 256 levels of thresholding.

The filter in the communications channel maximizes use of bandwidth with a minimum of inter-channel interference.[1] The ultimate filter has a brick-wall response and linear phase in its passband. But such filters don't exist at cutoff frequencies that can be used by engineers creating communications systems.

To support today's precise algorithms, the communication system's filtered digital channel requires excellent linear-phase performance, low jitter, and more attenuation in the adjacent channel than a Bessel filter can provide. In addition, testing these channels

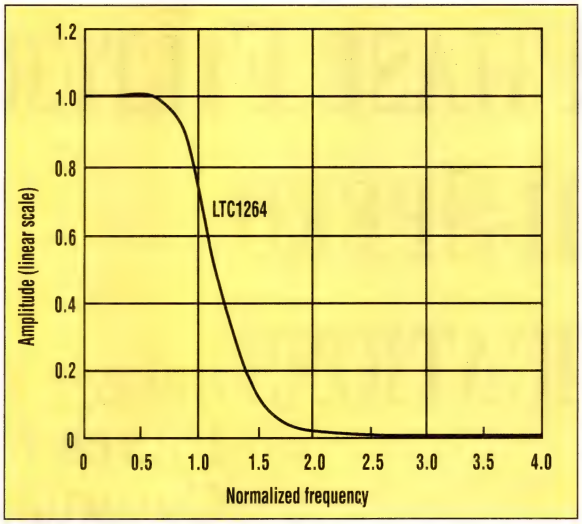


1. THE THEORETICAL brick-wall filter has a frequency response that's flat, and has no ripple in the passband up to the cutoff frequency (f_c). Then it rolls off to infinite attenuation at the beginning of the stopband (f_s).

is a challenge to filter designers who, unlike communications engineers, often don't have access to a plethora of test equipment. This article will provide a brief introduction to data-communications principles, and then discuss proper filtering to achieve the maximum amount of data into the minimum amount of valuable bandwidth real estate.

Transmission of data in a given bandwidth channel is more efficient when as many bits/s as possible can be transmitted through this channel. Shannon theorems show that the theoretical data-rate limit is the transmission of f_s symbols in a bandwidth (BW) of only $f_s/2$ Hz. Therefore, a binary transmission in which one symbol contains one bit, f_b (the number of bits per second) is equal to the symbol rate f_s. For M-ary systems, such as four-level PAM, each transmitted symbol contains n information bits (where $n = \log_2 M$). The symbol rate is then $f_s = f_b/n$. An M-ary system contains M voltage levels. While a binary system has two levels, an $M = 8$ system has eight levels. A two-level system can detect only 1 and 0, but higher level systems of PAM threshold in more than one place and therefore transmit more information in a given bandwidth.

Consider an example where it's required to transmit a 100-kbit/s source (f_b). Theoretically, this could be accomplished with a channel bandwidth: $BW = f_s/2 = f_b/2 = 50$ kHz. With the aforementioned four-level PAM scheme, the channel bandwidth reduces to 25 kHz $= f_s/2 = f_b/4$. This type of encoding is used by many types of digital communications systems. The trade-offs boil down to bandwidth versus encoding complexity. If the previously mentioned 100-kbit/s source must be passed in a bandwidth of 6.25 kHz $= f_s/2 = f_b/16$, it follows that 16-level PAM, or an equivalently dense packing scheme must be used. Multilevel and multiphase signals dictate that the filter be linear phase (to preserve pulse integrity in the time domain), while providing as much roll-off in the stopband as possible. More on these topics is included in the eye-diagram discussion later in the article.[2]



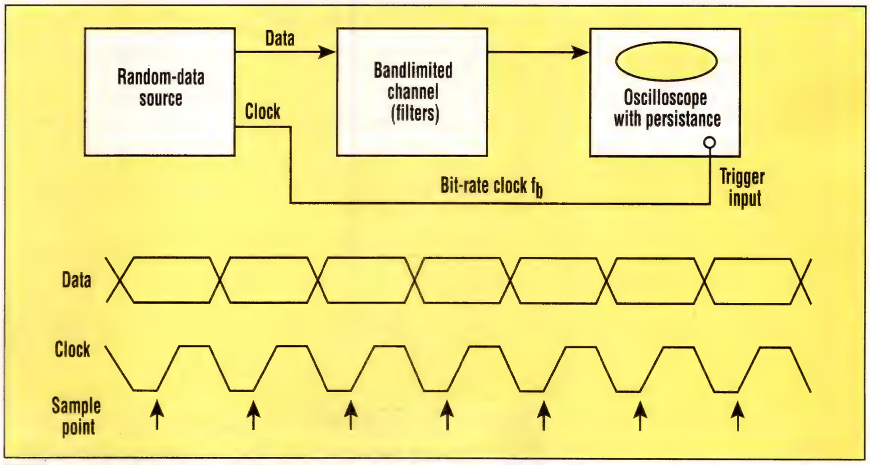
2. THIS PLOT SHOWS the amplitude response of the LTC1264-7 filter, which operates to 250 kHz.

The channel with bandwidth $f_s/2$ Hz is the brick-wall filter *(Fig. 1)*. A brick-wall filter has a frequency response that's flat (or 0 dB), with no ripple in the passband to the cutoff frequency (f_c). Then, it rolls off to infinite attenuation at the beginning of the stopband f_s. The brick-wall filter is only theoretical, thus $f_c = f_s$.

This brick-wall filter is the ideal channel that all filter designers strive for *(see "Filters for data communications," p. 92)*. Slight amplitude-response differences exist between Linear Technology's LTC1264-7 filter and Feher's alpha = 0.5 filter[3] (Kamilo Feher is a recognized authority in the field of digital communications). Alpha is the roll-off factor—alpha = 0 is the brick-wall filter and alpha = 1 implies twice the theoretical bandwidth requirement. The LTC1264-7 operates to 250 kHz *(Fig. 2)*. Other filters in the Linear Technology family operate on limited supply current: the LTC1164-7 uses only 4 mA of supply current while operating at corner frequencies to 2. kHz. The LTC1064-7 will operate to 100 kHz. The eye diagrams for these filters show them to be close to those of Bessel filters, but with better attenuation in the stopband.

An additional criteria for data-transmission filters (which they didn't tell you in college) is linear-phase response. Linear phase means that each frequency passing through the filtered channel will be delayed in time linearly according to its frequency. Higher frequencies have smaller delays (time). The group-delay specification illustrates this phenomenon with a plot of the delay of the group of frequencies versus frequency. The objective of a group delay plot is to have a flat line representing the situation where all frequencies are delayed the same amount of time.

Group delay is an important characteristic in digital-data-transmission applications because a filter with flat group delay passes a square wave with little distortion. Linear Technology's Better-than-Bessel filters compromise phase lin-



3. AN EYE-DIAGRAM generation system consists of a random-data source and an oscilloscope with persistance and a trigger input.

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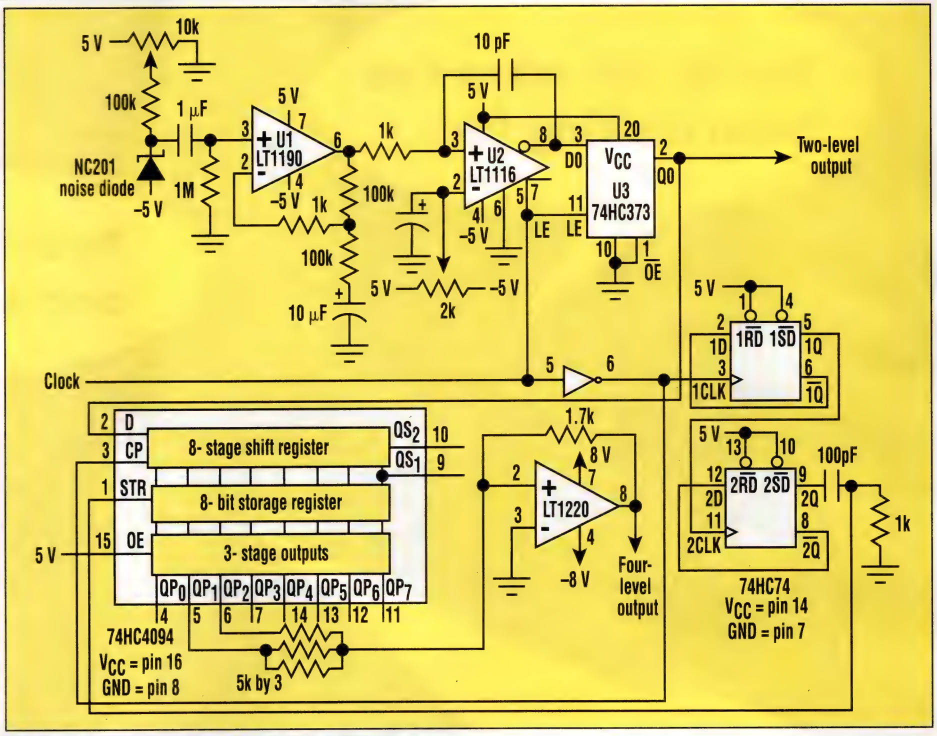
earity outside the passband to achieve more amplitude attenuation in the stopband. Kamilo Feher notes that for data transmission, filters should be linear in phase to their –10-dB amplitude points in the filter's transition region. The Dash 7 filters meet this criteria.



4. THE DATA-GENERATION circuit is actually a noise source sampled by a very fast comparator. The comparator outputs a random pattern of 1s and 0s.

Because the perfect, low-passed transmission channel doesn't exist, there must be a means by which to evaluate channel quality. That method is the eye diagram. The eye diagram is generated by supplying random data to the filters under test *(Fig. 3)*.

Symbols transmitted through a theoretical channel (Nyquist) have no degradation in amplitude response. Therefore, the measured eye-diagram opening of a real channel graphically shows the quality of the transmission channel, including the low-pass filter inserted in the transmission path. The degradation in the eye opening is directly related to intersymbol interference (the interference during the detection of one symbol in the presence of another), and thus is a measure of the system's bit-error rate.[1]

The test for measuring channel quality usually includes a digital oscilloscope configured to capture eye diagrams, or perhaps a dedicated digital-transmission analyzer. These pieces are costly and may not be available to the small or startup business. An empirical method of channel quality can done with the setup shown here, and, if more data is required, a bit-error-rate (BER) tester can be bought or rented.

A pseudorandom generator circuit feeds digital codes to the eye-generation setup shown in Figure 3. The generator circuit is actually a noise source sampled by a very fast comparator *(Fig. 4)*. The comparator outputs a random pattern of 1s and 0s.

A noise diode (NC201) is filtered and amplified by the LT1190 high-speed operational amplifier (U1). The output feeds the LT1116 (U2), which is a 12-ns, single-supply, ground-sensing comparator. A 2-kΩ potentiometer at the inverting input of the LT1116 sets the comparator's threshold so that a quasi-equal number of 1s and 0s are output. U3 latches the output from U2 so that the output from the comparator remains latched throughout one clock period. The two-level output is taken from U3's Q0 output.

The additional circuitry shown in the schematic lets the circuit output

FILTERS FOR DATA COMMUNICATIONS

The perfect filter for data communications, if it could be implemented, would be Feher's brick-wall, linear-phase, flat-group-delay, alpha = 0 filter. Unfortunately, that type of ideal filter can't be built.

Linear Technology offers an option to the unattainable filter with its LTC1064/1164/1264-7 "Better-than-Bessel" filters. These are 6th-order low-pass filters with a 2nd-order all-pass (phase-equalizing) section. The filters are contained in a 14-pin DIP or 16-pin SOL package. Each product includes the resistors needed to program the response of the switched-capacitor-filter sections included on the die.

The Dash 7 filters were designed by making them "Better Than Bessel." In other words, the low-Q Bessel response was modified to incorporate a notch or zero in the stopband to pull down the amplitude response just outside the filter's passband. This increases the attenuation from the Bessel's –14 dB at 2X cutoff to –28 dB for the LTC1264-7 (also at 2X cutoff).

The LTC1064-7 and LTC1164-7 filters have even better stopband performance (–34 dB at 2X cutoff). While this increased attenuation has little effect on the eye diagram, it increases the attenuation of the carrier signal without degrading the data that's superimposed on this carrier. This means better (that is, lower) bit-error rates for the same bandwidth channel.

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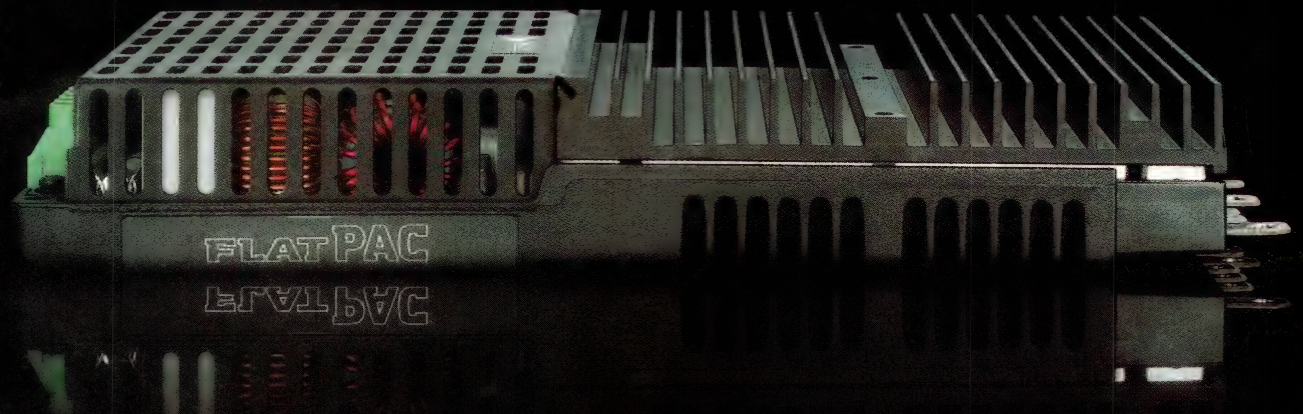

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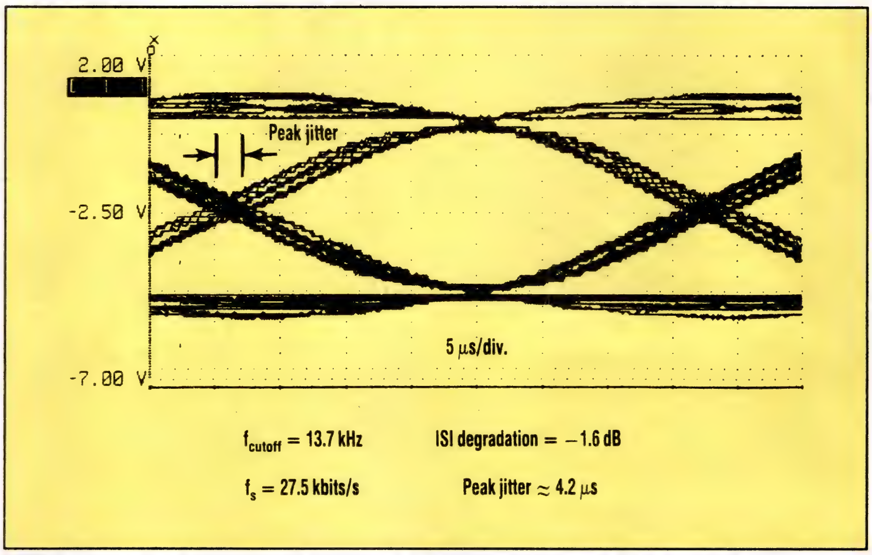
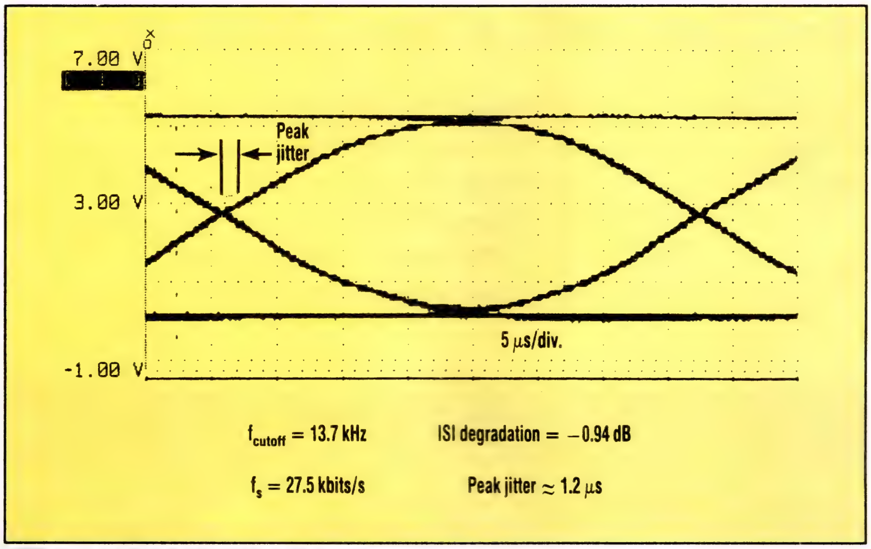
four-level data for PAM testing. Random data from the two-level output is input to a shift register, which is reset on every fourth clock pulse. Resetting the data ensures that it doesn't ripple through the register. To properly test a communications channel, data must slew to any conceivable state (and thus be random). Therefore, data must be able to go from a 0 state to a 3 state, as well as from a 0 to a 1. To do this in a truly random fashion, the register loaded with data must be read out and reset. This prevents the data from rippling through the shift register.

The output from the shift register is weighted by the three 5-kΩ resistors, and then summed into the LT1220 op amp from which the output is taken. The filter network between the 74HC74 output and the 74HC4094 strobe input ensures that the output data is correct.



6. COMPARING THE LTC1064-7 BETTER-THAN-BESSEL switched-capacitor filter with the Bessel filter reveals a slight increase in peak jitter over the Bessel. But it yields a 28-dB improvement in stopband attenuation versus the LTC1064-3 at two times the cutoff frequency.

Eye-diagram testing on three filters that might be used to filter a communications channel reveals some interesting data. Consider, for example, the LTC 1064-3 8th-order switched-capacitor filter with on-chip resistors, which is set to produce a response the same as that of a traditional Bessel filter *(Fig. 5)*. Note the almost perfect eye opening response and a lack of jitter at the half-level transition point. The Bessel filter is used as the model to which all other filters are compared in the eye-diagram (time-based) analysis. Comparison in the frequency domain is another matter.



5. AN EYE DIAGRAM for the LTC1064-3 Bessel filter shows a near-perfect eye-opening response and a lack of jitter at the half-level transition point.

The LTC1064-7 Better-than-Bessel switched-capacitor filter has superior stopband performance when compared to the Bessel filter (by 28 dB at two times the cutoff frequency) *(Fig. 6)*. However, nothing comes without cost. Here, the payoff is that the LTC1064-7 is linear in phase through its passband, but the Bessel filter is linear in phase to two times its cutoff frequency. The purveyors of the digital-communications ethic say, "Not to worry! A filter must be linear in phase only through its passband."[4] Note that the primary difference in the eye diagram of the filter in Figure 6 as compared to the Bessel filter is a slight increase in peak jitter.

The eye diagram of the Butterworth filter shows that not only does it have lots of jitter, but its eye isn't as open as the LTC1064-3 and LTC1064-7 filters *(Fig. 7)*. If a digital system switches at the midpoint in the two-level eye diagram, the BER will be higher for the eye diagram with the smaller eye opening. The calculation of intersymbol interference degradation due to channel or filter imperfections is a measure of degradation in BER. It's calculated as: ISI degradation = 20 log(actual eye opening/100% eye opening).

Testing communications channels using the eye diagram yields good results without having to resort to exotic instrumentation. Results of the show similar eye openings for the Bessel filter and the Better-than-Bessel filters. However, the jitter specifications are slightly improved by using the traditional Bessel filter.

The untold tale is in the frequency domain, where the LTC1064-7 has superior stopband attenuation, thus resulting in better attenuation of the carrier (at 27.5 kHz for the three eye diagrams shown in this article). This translates to better bit-error rates. The user must trade off ISI degrada-

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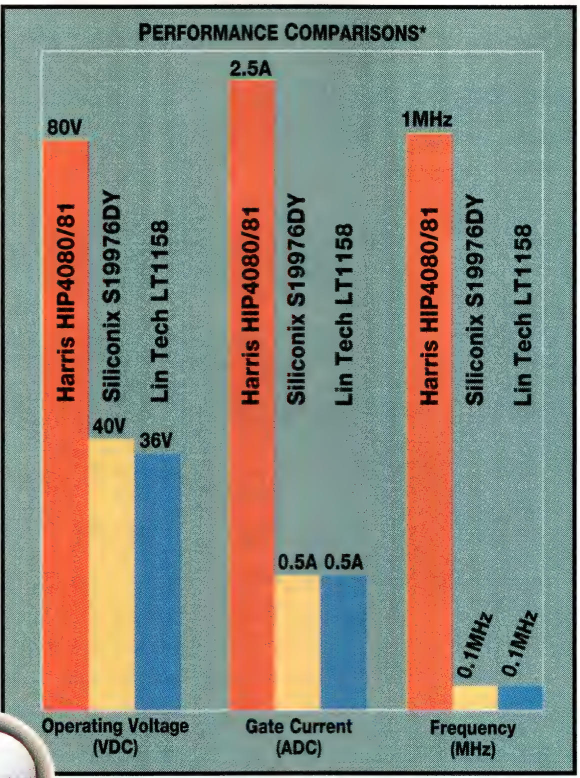

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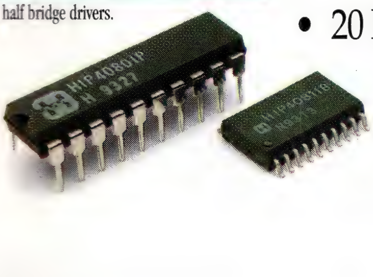

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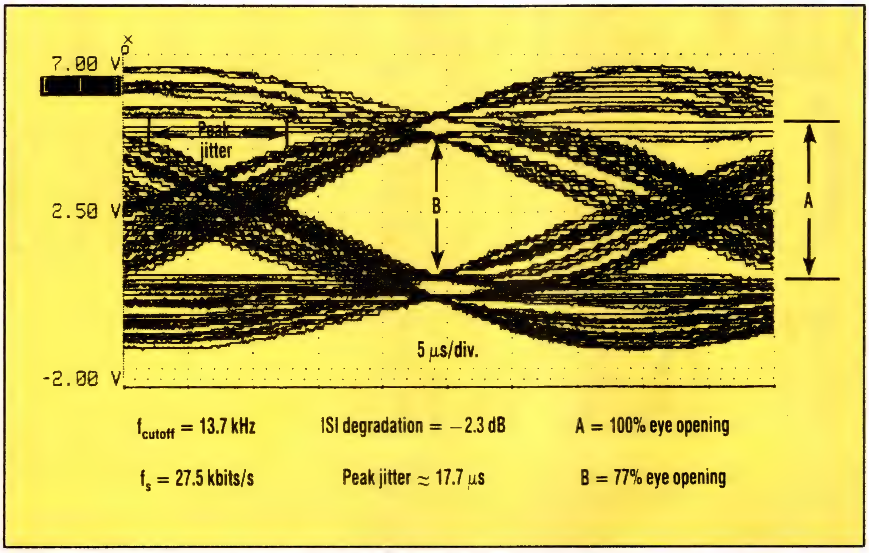
tion, jitter, and stopband attenuation to ensure the best channel performance. In addition, remember that the eye diagrams shown here are for two-level systems (0 and 5 V). For M-level systems, increased spectrum efficiency means that greater signal-to-noise ratios are required.☐

Parts of this article were excerpted from Linear Technology's Application Note 56.



7. THIS BUTTERWORTH FILTER eye diagram shows that it has a great amount of jitter, and its eye isn't nearly as open as the LTC1064-3 and LTC1064-7 filters.

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1. Feher, Kamilo. *Digital Communications: Microwave Applications*, Englewood Cliffs, NJ: Prentice-Hall Inc., 1981.
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4. Massey, John. Telephone conversation with Electronic Innovators Inc., Fairfax, Va., June 1992.

Richard Markell, applications manager at Linear Technology, holds a BA in electro-optics from San Jose State University, Calif.

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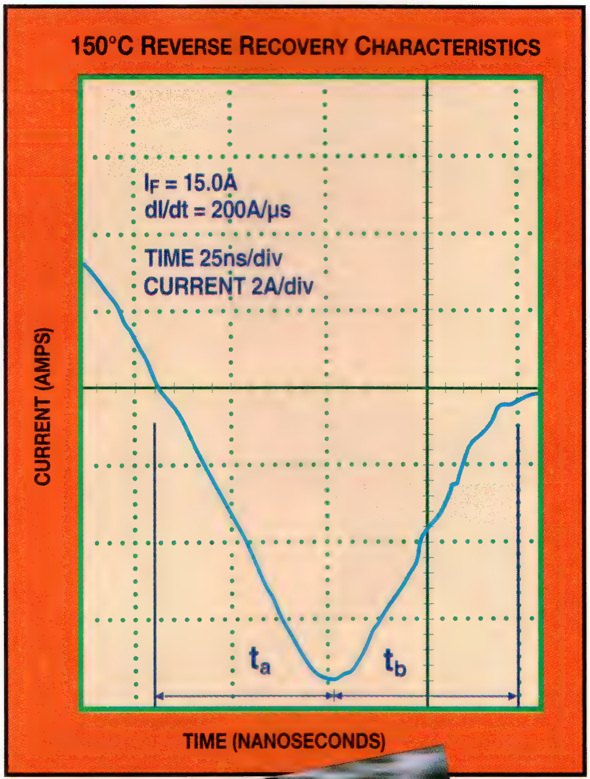

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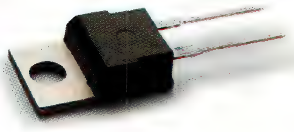

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CIRCLE 520

HIGH-EFFICIENCY BATTERY CHARGER

BRIAN HUFFMAN
Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035; (408) 954-8400.

High-efficiency battery-charger circuits are essential in laptop, notebook, and palmtop computers: they dissipate less power, and thus allow the use of surface-mounted components in the charger circuitry. Lower-efficiency solutions can require through-hole components, which increase board space, complicate pc board layout, and possibly exceed maximum height requirements.

The circuit shown *(Fig. 1)* can charge 4 NiCd cells at a 1.3-A fast charge or a 100-mA trickle charge with efficiency exceeding 90%. It can be easily modified to handle up to 8 NiCd cells.

Looking more closely at the setup, an LTC1148 is used in a step-down configuration to control the charge rate. The LTC1148 is a synchronous switching-regulator controller that uses a constant off-time current-mode architecture to drive external complementary power MOSFETs.

When the 1148's P-Drive output pulls the gate of Q1 low, the p-channel MOSFET is turned on, thus connecting one side of inductor L_1 to the input voltage. During this period, current flows from the input through Q1, through the inductor, and then into the battery.

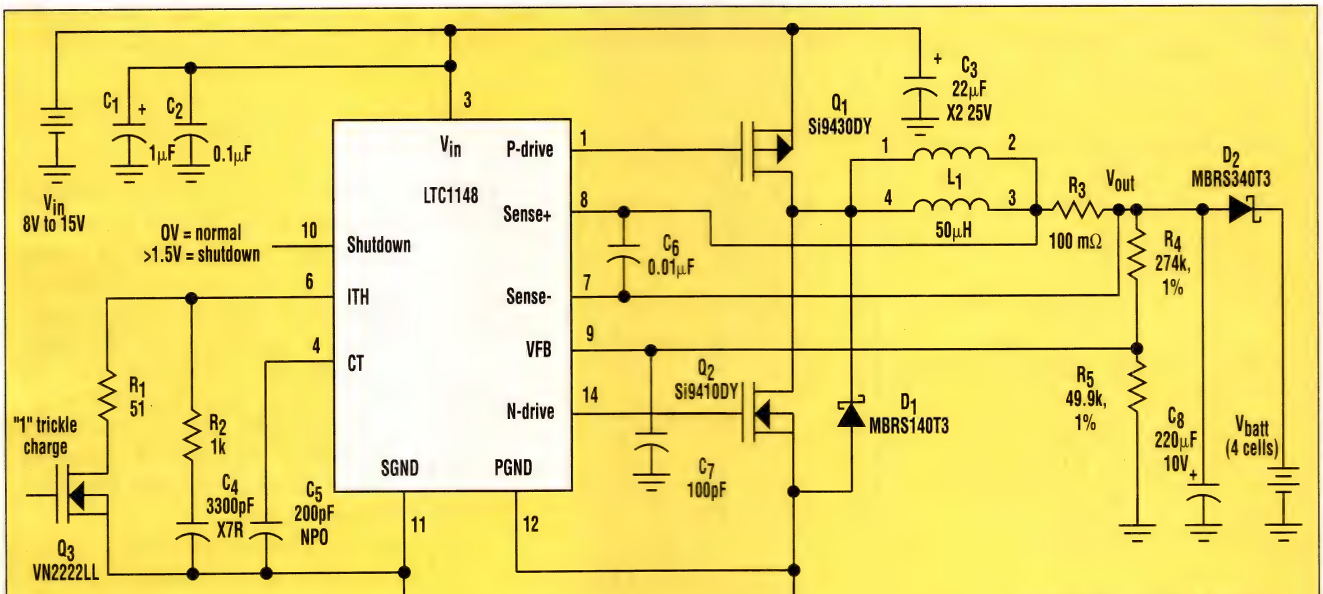
When the P-Drive pin goes high, Q1 is turned off. Then the voltage on Q1's drain drops until the clamp diode is forward-biased. The diode conducts only for a very short period of time, until the LTC1148's internal circuitry senses that the p-channel is fully off, preventing the simultaneous conduction of transistors Q1 and Q2. As a result, the N-Drive output goes high, turning on Q2 and shorting out D1.

Now the inductor current flows through the n-channel MOSFET (instead of through the diode), increasing efficiency. This type of switching architecture is known as synchronous rectification.

During the fast-charge interval, the resistor-divider network (R_4 and R_5) forces the LTC1148's feedback pin (VFB) below 1.25 V, causing the LTC1148 to operate at the maximum output current. Current is sensed by R_3, which is a 100-mΩ resistor, and set at approximately 1.3 A (130 mV/$R_3 \approx$ 1.3 A).

When the batteries are disconnected, the error amplifier servos the feedback pin to 1.25 V, limiting the output voltage to 8.1 V. Diode D2 prevents the batteries from discharging through the divider network when the charger is shut down. In shutdown mode, less than 20-μA of supply current is drawn from the input supply.

The dual-rate charging is con-



V_{OUT} = 1.25 V × (1 + R_4/R_5) = 0.1 V

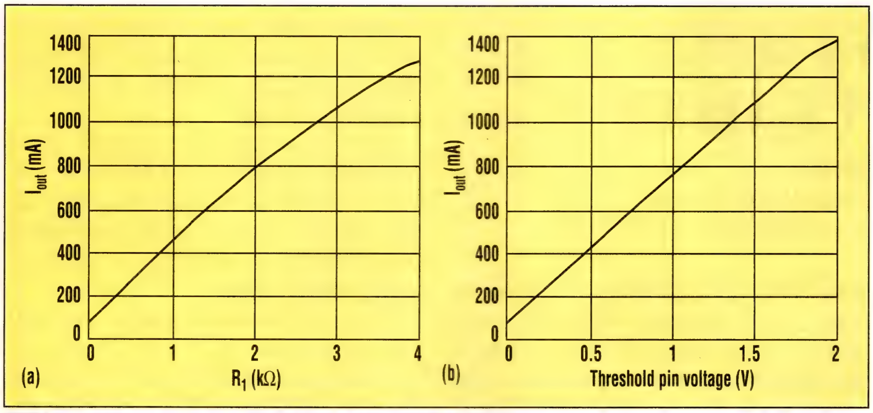
Fast charge = 130 mV/R_3 = 1.3 A

Trickle charge = 100 mA

C_1 = (TA)
C_3 = AVX (TA) TPSD226K025R0200
C_8 = AVX (TA) TPSE227M010R0100
Q_1 = Siliconix PMOS
Q_2 = Siliconix NMOS

D1, D2 = Motorola Schottky
R3 = KRL SP-1/2-A1-0R100J; Pd = 0.75 W
L1 = Coiltronics CTX50-4; DCR = 0.175; IDC = 1.350 A; KoolMu Core
All other capacitors are ceramic.

1. FOUR NiCd CELLS can be charged at a 1.3-A fast charge or a 100-mA trickle charge with efficiency exceeding 90%. The circuit uses an LTC1148 in a step-down configuration to control the charge rate.



2. THE LTC1148'S OUTPUT CURRENT is shown as a function of trickle-charge set resistance, R_1, (a), and as a function of the threshold pin voltage (b).

trolled by Q3, which can be toggled between a fast charging rate and a trickle charge for keep-alive. The trickle charge rate is set by resistor R_1. Figure 2a illustrates the selection of R_1 for a given trickle-charge output current.

The trickle charge current can also be varied by using an op amp to force the threshold pin voltage within it 0 to 2 V range. Figure 2b shows the output current as a function of the threshold pin voltage.☐

Brian Huffman is now with National Semiconductor Corp., Santa Clara, Calif., (408) 721-8277.

CIRCLE 521

ATTENUATOR DESIGN EQUATIONS

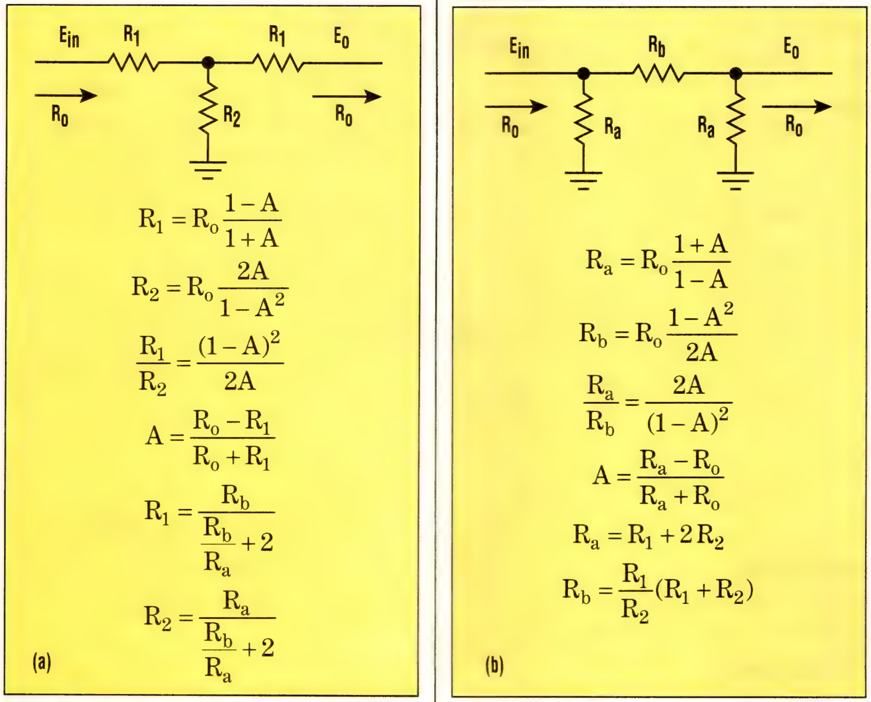
PATRICK H. CONWAY
28361 Plainfield Dr., Rancho Palos Verdes, CA 90274.

Deriving equations to find component values for a given network can be quite a tedious task for engineers who have been away from school for several years. Textbooks or handbooks usually don't include such equations.

One book in particular, the Sams-ITT *Reference Data for Radio Engineers* (sixth edition, 1975), does include some helpful tables, but they are not general enough.

In the figure, the equations are given for the resistor values of symmetrical "T" and "π" attenuators at an impedance level of R_o Ω as a function of the voltage gain, A ($A = E_o/E_{in}$ for $0 < A < 1$).

Expressions for the ratios of the resistor values are also given, because they can be useful in finding one resistor value as a function of the other. Equations for network attenuation and "T" to "π" transformation equations also are given.☐



(a)

$$R_1 = R_o \frac{1-A}{1+A}$$

$$R_2 = R_o \frac{2A}{1-A^2}$$

$$\frac{R_1}{R_2} = \frac{(1-A)^2}{2A}$$

$$A = \frac{R_o - R_1}{R_o + R_1}$$

$$R_1 = \frac{R_b}{\frac{R_b}{R_a} + 2}$$

$$R_2 = \frac{R_a}{\frac{R_b}{R_a} + 2}$$

(b)

$$R_a = R_o \frac{1+A}{1-A}$$

$$R_b = R_o \frac{1-A^2}{2A}$$

$$\frac{R_a}{R_b} = \frac{2A}{(1-A)^2}$$

$$A = \frac{R_a - R_o}{R_a + R_o}$$

$$R_a = R_1 + 2R_2$$

$$R_b = \frac{R_1}{R_2}(R_1 + R_2)$$

EQUATIONS ARE PROVIDED for the resistor values of symmetrical "T" and "π" attenuators at an impedance level of R_o Ω as a function of voltage gain A, as well as equations for transformation between the two types.

CORRECTION

This Idea for Design describing attenuator design equations appeared in the May 16 issue, but with an obvious omission: The design equations were inexplicably omitted from the illustration. We therefore are reprinting the Idea in its entirety.

The editors extend apologies to author Patrick H. Conway and to all readers of the Ideas for Design section.

MORE IDEAS AHEAD

This issue marks the beginning of an expanded Ideas for Design section, which means we will need more innovative ideas from our engineer-readers. Send your Ideas for Design to:

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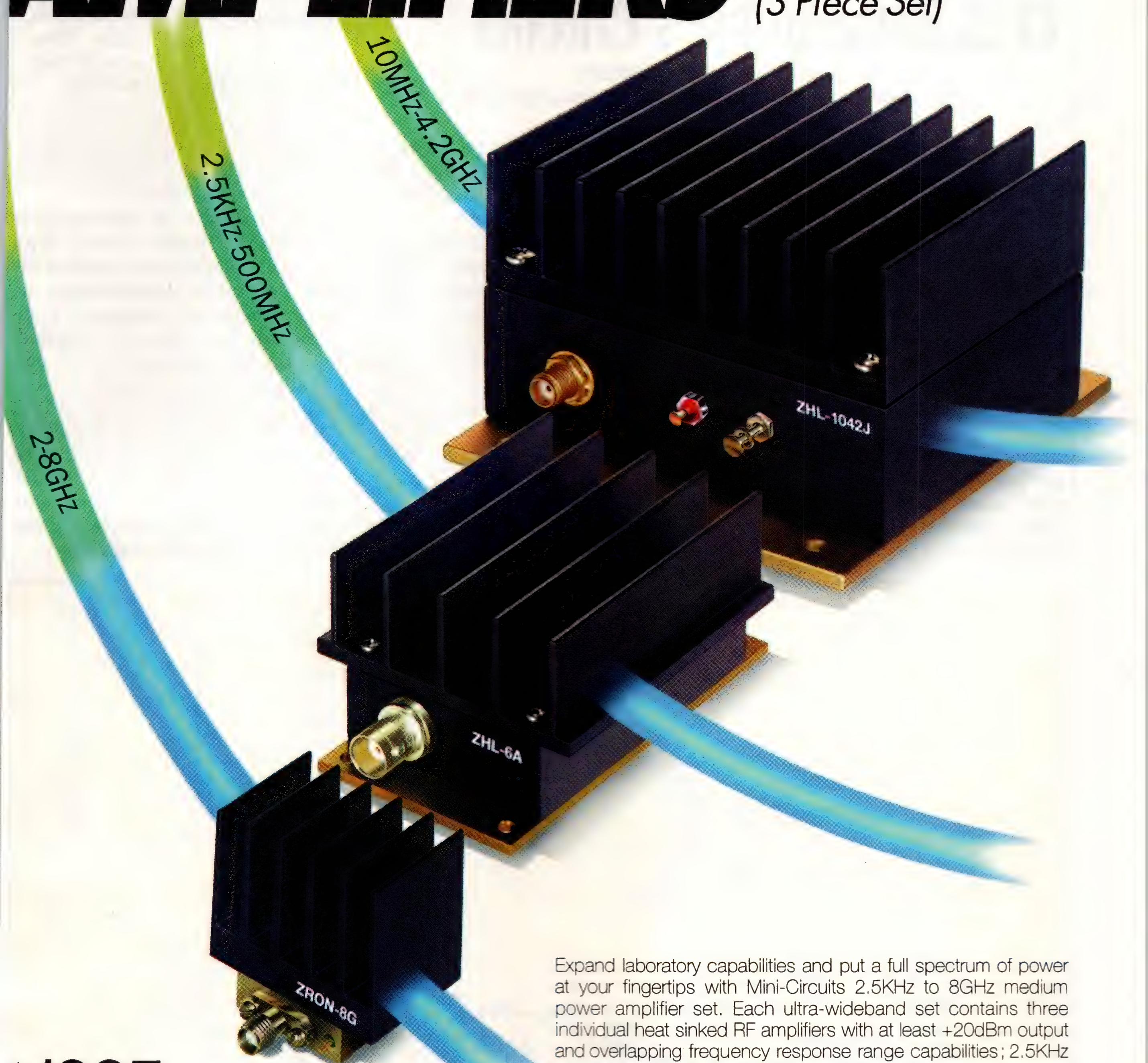

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CIRCLE 522

ACCELERATION-TO-FREQUENCY CIRCUIT

DAVID QUINN and CHARLES KITCHIN
Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887.

Acceleration, the change in an object's velocity, is a physical phenomena that often needs to be monitored. Accelerometers are used to measure motion, shock, vibration, inclination (by measuring the Earth's gravity), velocity (by integrating the accelerometer's output), and position (by double integration).

The figure depicts a circuit that has an output frequency which varies with applied acceleration. A small monolithic accelerometer in a TO-100 package directly converts any applied acceleration into a voltage that's extremely linear over a 0-g to ±50-g range. The voltage at pin 8 of the ADXL50, which is +1.8 V with no acceleration, changes by 19 mV for each 1 g (positive or negative) of applied acceleration.

An on-chip buffer amplifier scales and offsets this to an output of ±200 mV/g at pin 9. This output voltage directly drives an AD654 voltage-to-frequency converter IC. The frequency output appears at pin 1 of the AD654. Zero g and scale-factor potentiometers permit this circuit to be trimmed to high accuracy. The circuit operates from a single +5-V power supply (or from a 9-V battery via a resistor and Zener diode).

Using the components shown in the figure and with the output connected to a small speaker, various rotational angles or slopes are able to be detected by the audible change in pitch from the speaker.

The circuit can be self-calibrated by using the Earth's gravity. With the accelerometer's tab pointed 90° to the vertical (i.e., to either side), the accelerometer will measure 0 g, allowing the 0-g offset to be adjusted. With the tab pointing down, its output at pin 9 will correspond to +1 g. If the accelerometer is rotated 180°, it will then measure –1 g. The difference in the readings, 2 g, can then be used to set the device scale factor. Offset and scale-factor adjustments should be repeated a couple of times to get the highest accuracy.☐

Send in Your Ideas for Design
Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

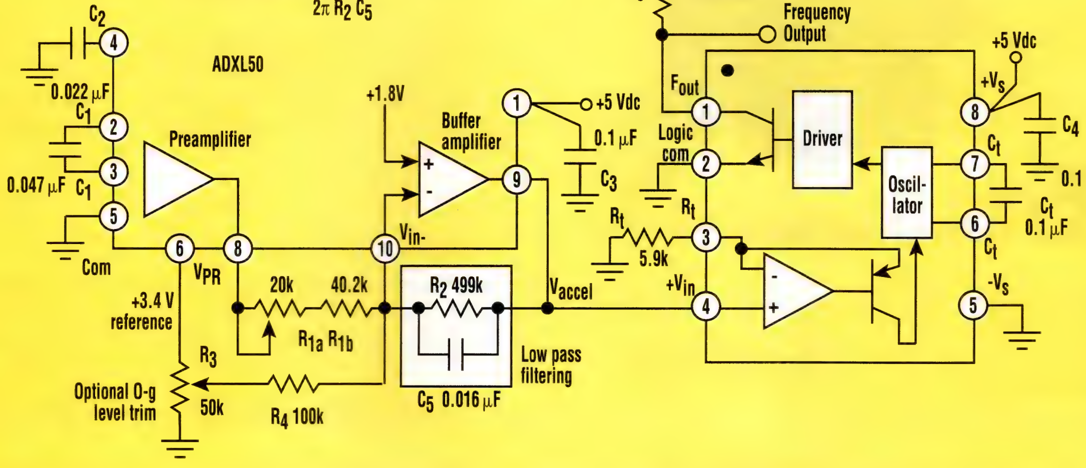
0-g frequency	SF	R_1 (Ω)	R_2 (Ω)	R_T (Ω)	C_T (μF)
10 Hz	10	20 k	1.89 M	1.8 k	10
100 Hz	10	52.7 k	499 k	1.8 k	1
100 Hz	100	20 k	1.89 M	1.8 k	1
1 kHz	10	184 k	174 k	1.8 k	0.1
1 kHz	100	52.7 k	499 k	1.8 k	0.1
1 kHz	1000	20 k	1.89 M	1.8 k	0.1
10 kHz	10	181 k	171 k	1.8 k	0.01
10 kHz	100	184 k	174 k	1.8 k	0.01
10 kHz	1000	52.7 k	499 k	1.8 k	0.01
100 kHz	10	198 k	1.8 k	1.8 k	0.001
100 kHz	100	181 k	17.1 k	1.8 k	0.001
100 kHz	1000	184 k	174 k	1.8 k	0.001

Design equations:

$$\text{0-g frequency} = \frac{0.18}{R_t C_t}$$

$$\text{Scale factor} = \frac{\Delta\,\text{frequency}}{g} = \frac{19 R_2}{1000 R_1 R_t C_t}$$

$$\text{3-dB acceleration BW} = \frac{1}{2\pi R_2 C_5}$$



OUTPUT FREQUENCY varies with applied acceleration in this acceleration-to-frequency converter. The ADXL50 accelerometer's preamplifier is driven by the device's internal micromachined sensor. The compact, low-power circuit is ideal for portable applications.

CIRCLE 523

RESISTOR L-NETWORK MATCHES IMPEDANCES

JOHN DUNN
181 Marion Ave., Merrick, NY 11566.

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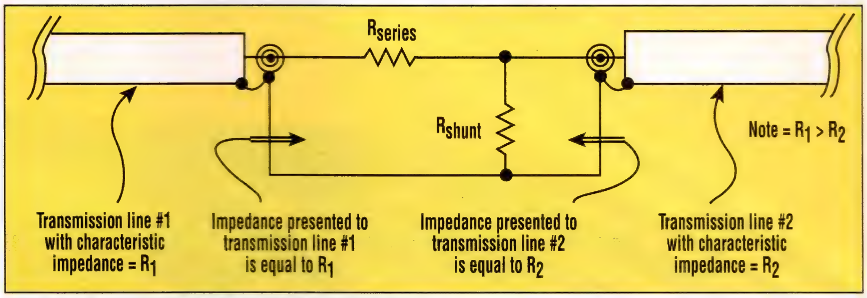
Yongping Xia, EBT Inc., 23600 Telo Ave., Torrance, CA 90505. His idea: *"Fuse Sounds Off When Overloaded."*

A resistor L-network can be a convenient impedance-matching circuit between two transmission lines of differing characteristic impedances. The two resistors are set to values calculated so that each line is presented with an impedance equal to its own characteristic impedance *(Fig. 1)*.


Rseries
Rshunt
Note = R1 > R2
Transmission line #1 with characteristic impedance = R1
Impedance presented to transmission line #1 is equal to R1
Impedance presented to transmission line #2 is equal to R2
Transmission line #2 with characteristic impedance = R2

1. A RESISTOR L-NETWORK can match impedances between two transmission lines of differing characteristic impedance. The two resistors are set to values that present each line with an impedance equal to its own characteristic impedance.

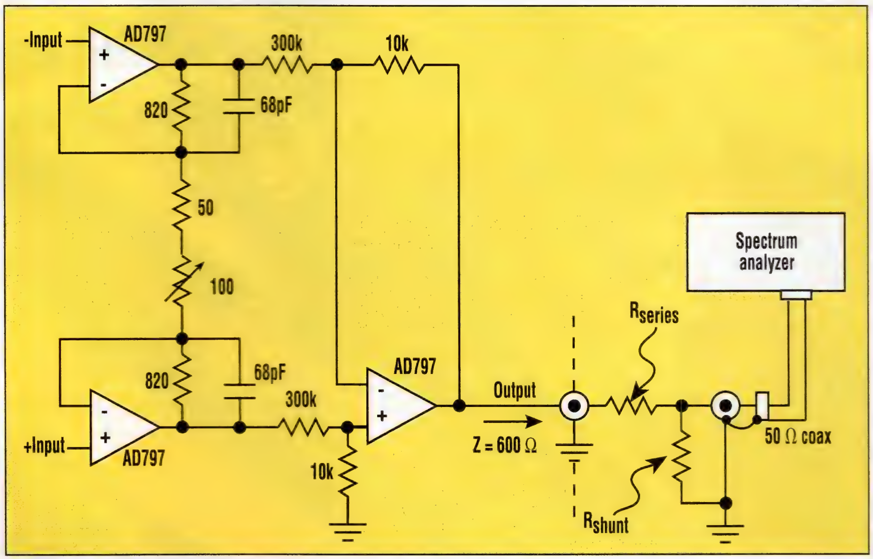
Consequently, with the acceptance of resistive loss, a nominal one-to-one VSWR can be maintained on each line.

Using the program given *(see the listing)*, the values of the resistors of an L-network can be found given the two transmission-line impedances that are to be matched.

In the examples shown in the listing, a 300-Ω-to-50-Ω L-network achieves 300 Ω from 54.77 Ω in parallel with 50 Ω, with that parallel combination then being in series with a resistance of 273.86 Ω. Conversely, the 50 Ω is achieved from a resistance of 273.86 Ω in series with 300 Ω, and that combined value is in parallel with the 54.77 Ω.

Users are then asked to specify the actual impedance values of interest, for which the required resistors are derived and printed along with the series and parallel combination results.

In addition, an L-network can help test amplifiers that are unable to support a low transmission-line impedance *(Fig. 2)*. A 600-Ω-to-50-Ω L-network makes it possible to test such an amplifier in a 50-Ω measurement system.



2. AMPLIFIERS THAT CAN'T SUPPORT low transmission line impedance can be tested by an L-network.

For really low noise devices like the AD797 shown, noise spectral density can be examined out to the amplifier's full bandwidth. (Of course, this second application of the L-network could also easily be served by a single buffering resistor alone, but it's satisfying to use the L-network for another purpose after going through the process of creating it.)☐

```
10 CLS:SCREEN 9:COLOR 15,1:GOTO 70
20 IF RIN>RL THEN GOTO 40
30 RA=RL:RL=RIN:RIN=RA
40 R2=RL*SQR(RIN/(RIN-RL)):R1=RIN-RL*R2/(RL+R2)
50 RX=RL*R2/(RL+R2)+R1:RY=(RIN+R1)*R2/(RIN+R1+R2)
60 PRINT USING B$;RX,R1,R2,RY,RY,RIN,R1,R2:RETURN
70 PRINT "save "+CHR$(34)+"padmatch.bas"+CHR$(34):PRINT
80 PRINT "save "+CHR$(34)+"a:padmatch.bas"+CHR$(34):PRINT:PRINT
90 A$=" Rin #1 = Rseries + Rshunt // Rload     "
100 A$=A$+"Rin #2 = (Rseries +  Rin #1) // Rshunt":PRINT A$:PRINT
110 B$="####.## = ####.## + (###.## // ###.##)     "
120 B$=B$+"##.## = (####.## + ####.##) // ###.##"
130 RL=50:FOR XX=1 TO 3:READ RIN:GOSUB 20:NEXT XX:DATA 75,300,600
140 PRINT:PRINT "New Rin #1 and Rin #2 ";:INPUT RIN,RL:GOSUB 20:GOTO 140
 save "padmatch.bas"
 save "a:padmatch.bas"
 Rin #1 = Rseries + Rshunt // Rload    Rin #2 = (Rseries +  Rin #1) // Rshunt
  75.00 =   43.30 + ( 86.60 //  50.00)    50.00 = (  75.00 +   43.30) //  86.60
 300.00 =  273.86 + ( 54.77 //  50.00)    50.00 = ( 300.00 +  273.86) //  54.77
 600.00 =  574.46 + ( 52.22 //  50.00)    50.00 = ( 600.00 +  574.46) //  52.22
 New Rin #1 and Rin #2 ? 90,75
   90.00 =   36.74 + (183.71 //  75.00)    75.00 = (  90.00 +   36.74) // 183.71
 New Rin #1 and Rin #2 ?
```

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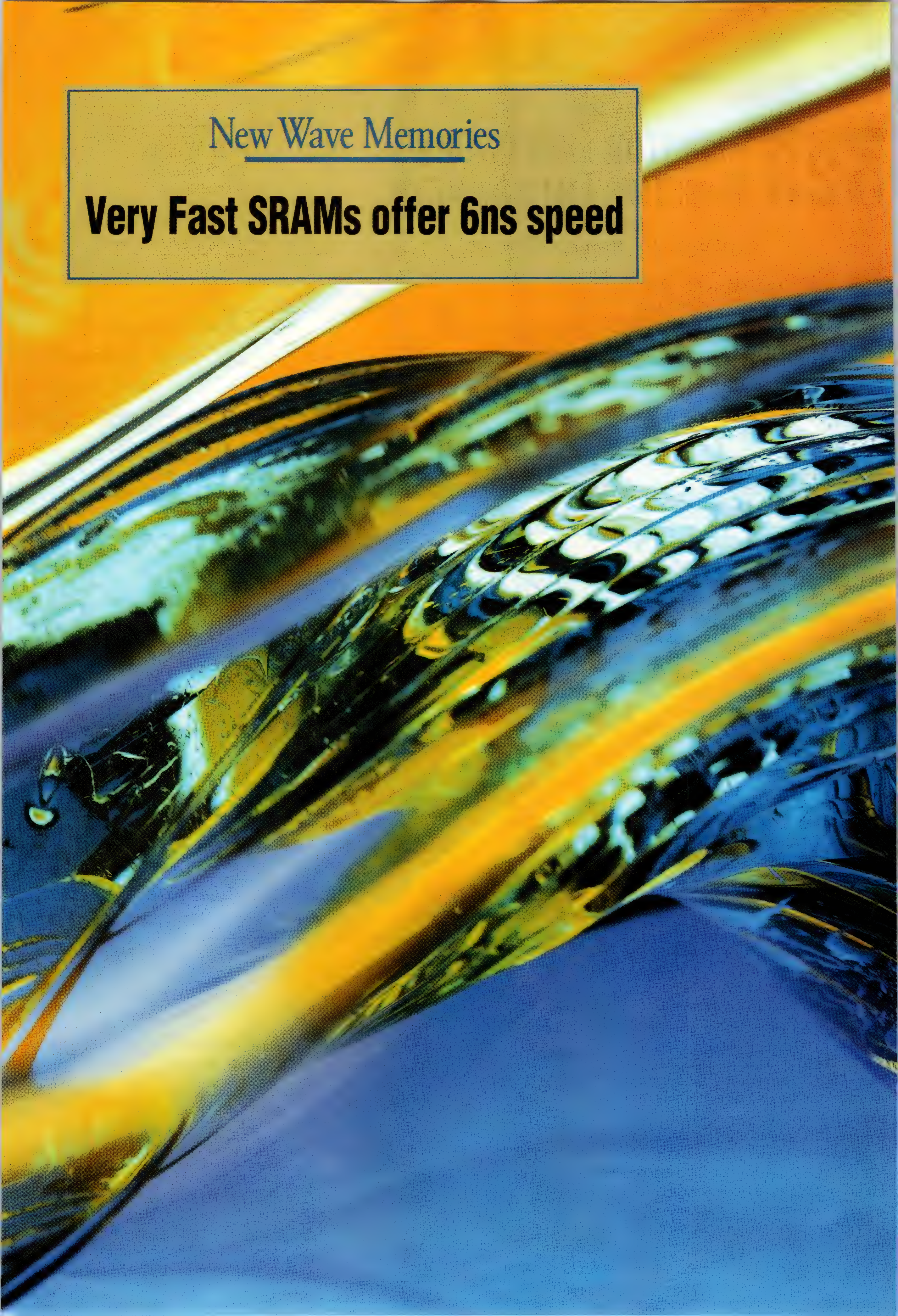

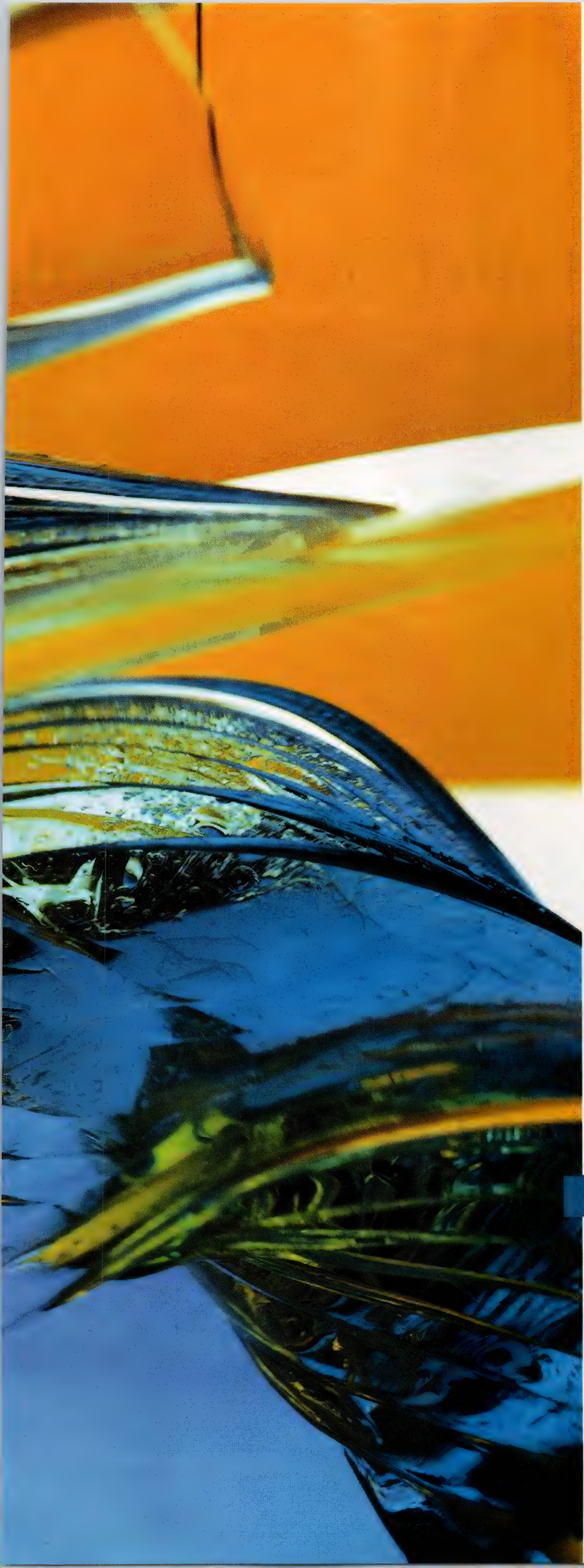

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μPD46259	32K x 9	
1M		
μPD461008	128K x 8	8,10ns (5V) 10,12ns (3.3V)
μPD461009	128K x 9	
μPD461016	64K x 16	10,12ns (3.3V)
μPD461018	64K x 18	

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4M		
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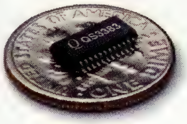

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ELECTRONIC DESIGN QUICKLOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

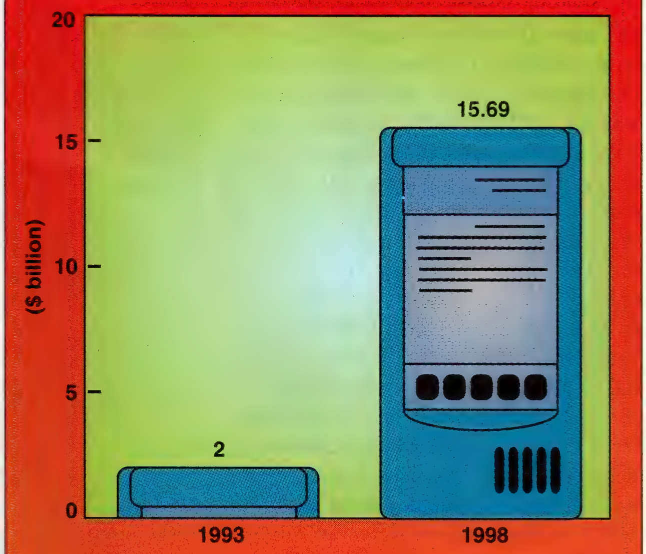
The U. S. market for wireless communication equipment and services will skyrocket from just over $2 billion last year to hit $15.69 billion in 1998. That's according to a report from The Information Network market research company, entitled *Wireless Communications: LANs, Cellular, MANs/ WANs, Pagers, and PBX.*

According to the Williamsburg, Va.-based researchers, key technologies driving the wireless wide-area networks (WAN) market are: the availability of radio modems that fit in pentop and laptop devices; wireless networks such as Ardis and RAM; and an increase in connectivity software and applications programs.

The researchers further predict that the U.S. market for wireless LANs will grow from $57 million last year to top $900 million in 1998, a compound annual growth rate (CAGR) of 73.7%. Wireless portable computers connected over packet switched networks are expected to grow from a $1.10 billion market in 1993 to be worth $9.60 billion in 1998, racking up compound annual growth of 67.1%.

Meanwhile, the Information Network forecasts that the U. S. market for pagers should increase from $638 million last year to be worth $1.13 billion in 1998; that year, nearly 35 million pagers expected to be at work alerting users to phone calls and messages.

U.S. MARKET SOARS FOR WIRELESS EQUIPMENT AND SERVICES



Source: The Information Network Williamsburg, Va., (804) 258-3738

QUICK REVIEWS

***A** Buyer's Guide to DSP Processors* compares 20 programmable digital signal processors from companies such as Analog Devices, AT&T Microelectronics, DSP Semiconductors, IBM, Motorola, NEC, SGS-Thomson, Star Semiconductor, Texas Instruments, Zilog, and Zoran. Authors of the guide, Berkeley Design Technology, report speed and power benchmark results for popular DSP chips. Speed and power benchmarks compare the performance of a dozen mainstream DSP ICs through 11 functions. The 670-page report has in-depth analysis of 23 DSP ICs and families, studies of DSP applications, a review of DSP technology, and a detailed processor comparison in table form. The report winds up with a look at industry trends and includes a glossary and index. The buyer's guide is $1850 for initial copies. Additional copies are $400. International prices are $100 more. A detailed brochure on the study is available from Berkeley Design Technology Inc., 39355 California St., Suite 206, Fremont, CA 94538; (510) 791-9100; fax -9127; e-mail: info@bdti.com. CIRCLE 461

***C**omputer Algorithms: String Pattern Matching Strategies*, edited by Jun-ichi Aoe, introduces string pattern matching stategies, describes the application and implementation of a variety of string-matching algorithms, and investigates problems and their solutions. Published by the IEEE Computer Society Press of Los Alamitos, Calif., the book begins with an introduction that describes the basic concepts of classification. The five chapters that follow present 15 papers illustrating further the classifications of string pattern matching. List price is $56. Contact the IEEE Computer Society Press, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720-1264. CIRCLE 462

***F**oundations of Parallel Programming: A Machine-Independent Approach* by Ted G. Lewis covers the design of parallel programs using a small number of fundamental constructs powerful enough to express any parallel algorithm. By using a simple pseudo-code notation for describing parallel programs, the book is language- and machine independent. List price is $60. For more information, contact IEEE Computer Society Press, 10662 Los Vaqueros Circle, P.O. Box 3014, Los Alamitos, CA 90720-1264; (714) 821-8380; fax -4641; e-mail number is cs.books@computer.org. CIRCLE 463

***F**rontiers of Scientific Visualization*, edited by Clifford A. Pickover and and Stuart K. Tewksbury, explores the use of scientific displays to produce art and visualization of various processes and scientific phenomena, including 16 pages of color, computer-generated illustrations. List price of the book is $34.95 (John Wiley & Sons, 605 Third Ave., New York, NY 10158-0012; (212) 850-6497; fax -6799). CIRCLE 464

QUICK NEWS

Developed as a standard for managing desktop computers, servers, hardware and software products, and peripherals, the Desktop Management Interface (DMI) specification has been finalized by the Desktop Management Task Force, Hillsboro, Ore. That will lead to the release of the software development kit for the DMI 1.0 release by mid summer of this year. The kit includes service layers for DOS, Windows and OS/2, sample management-information format (MIF) files, and other development tools. And, for DMI implementations for future and other existing operating systems, the DMTF will also make core DMI technology available to operating-system vendors in mid 1994. For PC users and LAN administrators, DMI-ready PC products will allow management of desktop resources in a consistent manner. That, in turn, will make PC systems and products easier to use, manage, and track, as well as simplify technical support and troubleshooting. Founding members of the DMTF include Digital Equipment Corp., Hewlett-Packard Co., IBM Corp., Intel Corp., Microsoft Corp., Novell Inc., SunConnect, and SynOptics Communications Inc. Vendors interested in obtaining the DMI 1.0 specification can contact the DMTF hotline at (503) 696-9300. *DB*

OFFERS YOU CAN'T REFUSE

Black Magic! Telecom Design Tricks assembles advanced design principles and practices for telecom power, ringing, and ISDN circuits, including 20 "cookbook" schematics. For a free copy, contact Cambridge Electronics Laboratories, 20 Chester St., Somerville, MA 02144-3005; (617) 629-2805; fax 623-1882; internet address: 62075697@eln.attmail.com. CIRCLE 465

The latest issue of the American Engineering Association's *American Engineer* discusses a Minnesota bill that would require employers to use inventions created by engineers in the company within a set period or to give the rights to the employee. The AEA urges engineers in favor of such legislation to write the authors of the bill, Sen. Kevin Chandler and Rep. Betty McCollum at the Minneosta State Capital Building, St. Paul, MN 55101. Yearly AEA membership starts at $30, including newsletters. For a complimentary copy, write AEA at P.O. Box 820473, Fort Worth, TX 76182-0473; (817) 431-1319.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ

President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Many comments on the number of hours you work in a week have come in electronically and by mail. The feedback suggests many of you work long and hard to get those new products to market. Some of the feedback on the hours worked in a week was anonymous—a first for this column. Have I struck a sensitive organizational nerve? I'm not here to judge the relative merits of working a 50-, 60-, 70-, or 80-hour week vs. the 40-hour discussion reference—that's up to you. But for change to take place, the management of commitment must be visible throughout your organization at all levels. You get the needed visibility from the resource-driven databases you maintain on each project.

Here's a true story that concisely puts many issues into perspectivet . . . I was skiing with an associate whose son, a software engineer, worked for the Big Software Company. His son reported that he was expected to work at least an 80-hour week, even more was better. For a period of almost two years, this youthful software engineer contributed to bring forth the firm's latest software release. His compensation was about $40,000 per annum.

At 80 hours per week, burnout resulted; this engineer had to make a change. Fortunately, he saw his situation in a unique way: He thought of his 80-hour-per-week, $40,000-per-year job as two 40-hour-per-week, $20,000-per-year jobs. This simple situational transformation set his mental wheels in motion. He first attempted to reduce the hours worked per week with his existing employer, and, for a variety of reasons, found that he was fighting a losing battle. He then decided to look for two jobs whose combined compensation would pay the same but that offered greater opportunity and personal satisfaction. For one of his 40-hour-per-week jobs, our young engineer went to work at a Lake Tahoe ski resort; for the other job, he does contract software development. There was a struggle from the beginning, but now our engineer works a combined total of about 60 hours a week and makes more money then he did before. The moral of the story—working people too hard burns them out and forces them into action. So what does this mean in a generalized situation?

Engineers do burn out and when they do there are no winners! It's in the best interest of the new product development organization to keep it from happening and it's in the best interest of the employee. Organizations and their engineers must create a win-win situation to sustain the flow of new products while satisfying basis human needs.

To spot potential burnout and to prevent its occurrence, create and maintain a new product development database. With a database, project teams know what is ahead, what has been accomplished, where to deliver their work, and the location of the big time-consuming problems. This information provides the focus necessary to direct energy into the critical few items necessary to project success at a particular point in time.

The concepts of the minimal serial network and determination of project timing by the application of resources to tasks makes overworking resources very visible. Seeing the potential problems leads to creative solutions! Once data is in the computer system, viewing how each resource works over time is very easy to accomplish. A resource histogram for each person is displayed and analyzed. Then adjust to best use resources.

The individuals allocating resources to tasks over time maintain control of the pace at which the project will proceed by the way they structure, estimate, staff, allocate, and run the project. With the project network in place, product can be delivered to market earlier simply by carefully applying resources to reduce the time needed to complete critical path items within the network. The decisions made in producing the database set the tone for the rate of work progress. A good plan provides a reasonable distribution of work across the entire team; everyone contributes his or her fair share and no one burns out.

Ron Kmetovicz's One-Minute Time to Market Self Assessment is available free to the readers of Electronic Design by contacting Time to Market at the address above.

graphical programming languages *have certain limitations when it comes to test development.* •*No one has figured out a way to let you create tests as powerful as the ones you're running now.* •*No one has figured out how to control every instrument you're likely to use.* •*No one has figured out a way to let you leverage your existing code.* •*If anyone ever figures this stuff out,*

there's going to be a big noise about it.

Ba

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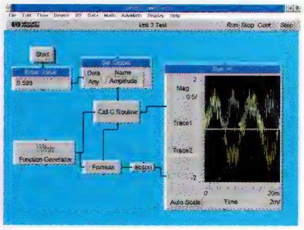
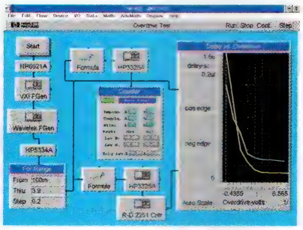


Standard language ties give you the flexibility to use existing code or create new C routines.



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If you have it, HP VEE supports it. The choice of instrument control is yours. In addition to more than 350 full-featured drivers that come standard with the software, HP VEE's Direct I/O lets you send any command to any instrument. If you need custom drivers, a built-in driver writer makes it easy to create custom drivers in minutes.

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READER SERVICE 213

QUICKLOOK

MY VIEW

...Tuesday is music day

BY FRANK J. BURGE
Director of Market Development for Electronic Design

When I was a senior in high school, twelve of us who hung around together had a club called the Boxcars AC. The AC stood for athletic club. One summer we organized a baseball team and even had a raffle to finance uniforms. Burke's aunt won the prize (a watch) because she bought more tickets than anybody. With a name like Boxcars AC, I don't think any of our benefactors really expected the raffle would be legit.

When we counted the proceeds, we decided to have a picnic rather than buy uniforms. So we got dates, rented a bus, loaded it up with beer, and headed for the Indiana Dunes. What a grand day it was. When we arrived at the Dunes, my buddy Gootch suggested we bury two cases of beer to keep them cool. It sounded like a good idea at the time but towards evening when we had run out of hootch, nobody could remember where we had buried the suds. Just as well. Forty-two years later Gootch tried to organize a search party since he claimed the location of the buried treasure had been revealed to him in a dream. Gootch is still a fruitcake.

On May 1 my wife's sister Lou collapsed and was airlifted from Bullhead City, Ariz., to a hospital in Las Vegas. When we arrived at the hospital late that afternoon, she was being kept alive with the usual life-sustaining paraphernalia. Early the next morning, she was pronounced brain dead. At the funeral service her five grandchildren, ranging in age from three to nine, sang her favorite song. It was a fitting end to a life filled with the music of young hearts.

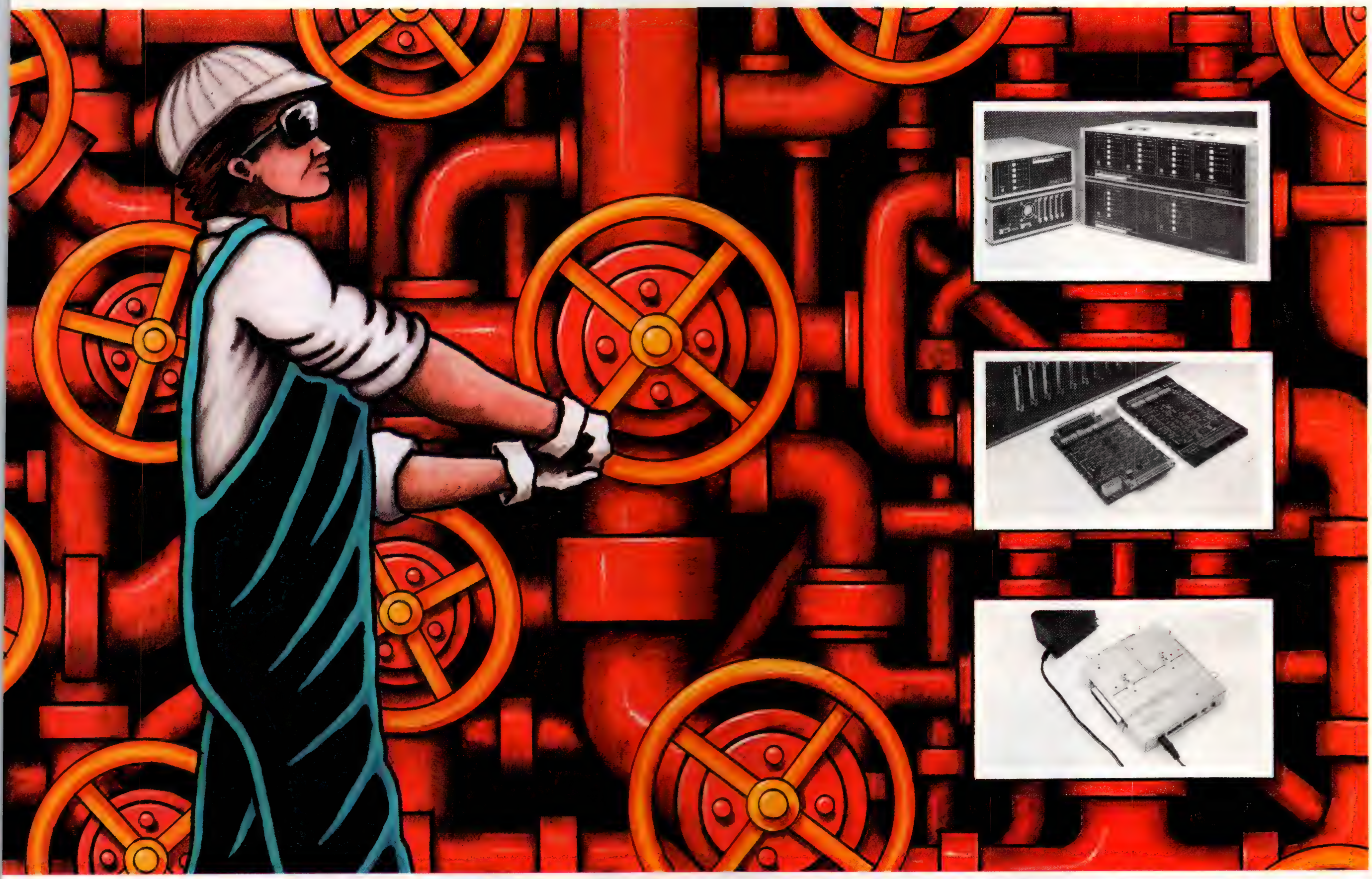
After the funeral service, the senior citizens of Laughlin, Nevada, hosted a luncheon for family and friends and there was more music, this time in the form of hugs and emotion. There are lots of loving people in Laughlin, but my guess is there are lots of loving people everywhere, except we're often too busy to notice. My wife Barbara is the youngest of six children. Now there are only two left: Barbara and her brother Frank, who lives in Hebron, Indiana. Time and the inevitable end game have a way of breaking up families and breaking hearts.

Looking back on my own life, enriched by so many loving people along the way, I couldn't help but ponder how time does fly. It seems like only yesterday we were furiously digging for the buried beer and laughing like crazy. That was music to my ears—a grand day indeed.

And at one time, the air was filled with music in our business, people caring for each other, mixing fun with hard work and sharing the good and the not-so-good times. But now, at least for many in our business, there is no music. Downsizing and the reengineering crusade have caused thousands to be tossed on the scrap heap. And thousands more are looking over their shoulders wondering if they'll be next. Others are trapped in boring jobs and feel stuck for lack of opportunity. So it's not surprising that in many camps paranoia has replaced caring and suspicion has overtaken laughter. People are just too busy to take the time to have lunch with a friend, or whistle or let loose with song or a dance or whatever nutso shtick suits the occasion. If there was ever a time for music, caring, and laughter, it is now.

My barber has an idea that he picked up from the popular "dress down" day—where on Friday everyone in the company dresses casually. My barber figures we ought to set aside Tuesdays as music day, loosen-up day. Make a face at a friend, hug a customer, pass out some high fives, bury a case of beer in the front lawn, or whatever. But loosen up and help folks have some fun. Mark it down, Tuesday is music day.

When You Need To Switch



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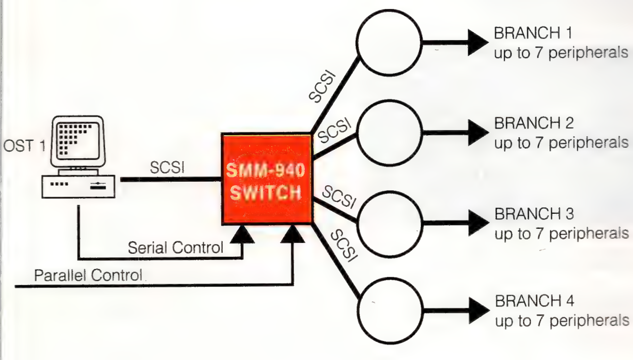
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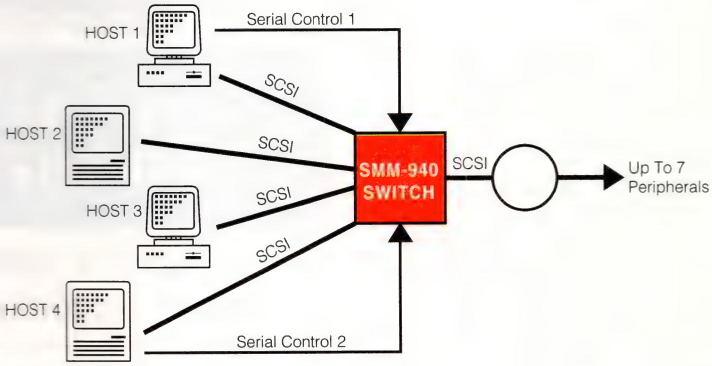

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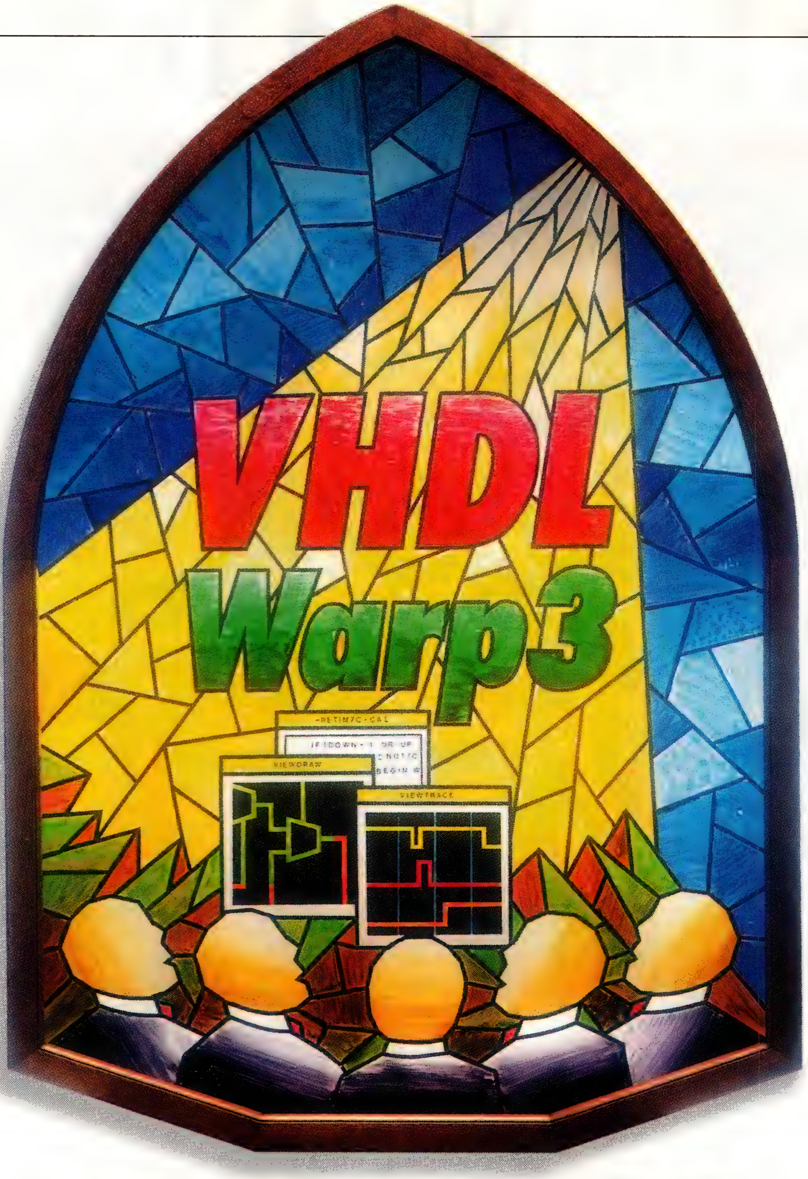

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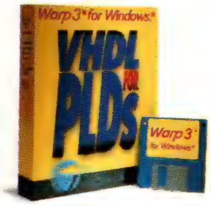

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CYPRESS

PEASE PORRIDGE

BOB'S MAILBOX

Dear Mr. Pease:

You owe a profound apology to approximately 600,000 radio amateurs in the United States for the remarks you made about them in your April Fool's Day piece in the April 4 Pease Porridge

You were right when you said "...ham radio guys are always inventing and building equipment so they're prime targets for pranksters." But you missed the mark a mile when you went on to describe how "many hams" built the 50-ohm dummy load described by Tom Kneitel in his 1969 article in *S9* magazine.

First of all, *S9* was a publication aimed at citizen's banders and ham wannabes, *not* at hams. The real ham publications available then were *QST* (the widely respected and often quoted journal of the American Radio Relay League), *73* (an independent magazine aimed largely at gadget builders), *Ham Radio* (a technically-oriented magazine written mostly by engineers), and *CQ* (written then, as now, for hams who like contesting and DXing).

Now you may not be aware of the difference between citizen's banders (CBers) and hams, so let me give you just a few of the highlights:

- In 1966, hams, even at the lowest beginning level, were required to pass federally supervised examinations covering technical subjects (resistors, inductors, and capacitors in series/parallel, resonance, antennas, etc.), governmental rules and regulations, propagation, and operating procedures. They also had to demonstrate the ability to send and receive Morse code at 5 words per minute. Higher-class amateur licenses had more difficult tests and faster code requirements (13 WPM or 20 WPM). CBers in 1966 only had to apply for a license. Today, hams are still rigorously tested before earning their licenses. CBers are not even required to have licenses.
- To obtain my Technician Class license (one step above bottom) back in 1959, I was required (among other things) to draw from memory the schematic of a push-pull twin triode power amplifier with link-coupled input and output; and cross-coupled neutralization. Could RAP have done that at age 17? Could he do it today?
- Hams are allowed to operate on any frequency within their many bands (some are hundreds of megahertz wide). CBers are allowed to operate on only 40 specific frequencies in the 27-MHz band.
- Hams are allowed to design and build their own equipment; CBers may buy only FCC type-accepted equipment. Hams may adjust and modify their equipment; CBers are not allowed to tamper with the circuits.
- Hams are permitted to transmit using up to 1500-W PEP output; CBers are limited to 10-W PEP.
- Hams are allowed to utilize many different modes of communications: AM, FM, PM, SSB, code, slow-scan TV, fast-scan TV, fax, teletype, packet data, and spread spectrum. CBers are permitted only voice, using AM or SSB.
- Hams are permitted to build and operate mountain-top VHF repeaters to extend the range of their handheld or mobile radios; CBers may not. Hams are allowed to design, build, launch, and operate their own satellites (there are several in orbit as we speak); CBers...well, sorry.
- Hams have gathered world-wide acclaim for selflessly donating millions of man-hours every year to provide the public with emergency communications in fires, floods, hurricanes, war, and earthquakes.

I could go on at length, but perhaps by now you get the idea. And while I suppose it's possible that a few hams might have been fooled by the *S9* article (just as at least one engineer was taken in by the BD-1 article), it seems unlikely that "many hams" would be taken in by a pretty obvious gag in a CB magazine. More likely, the victims were naive CBers who had never heard of a dummy load.

BARRIE G. BRITTON
Amateur Radio K0WWG
Riverside, Ca.

Okay, probably I should have said "several CB guys and a few hams" were fooled into building the dummy load. I'm sorry!—RAP

Dear Mr. Pease:

Your "Pease Porridge" column in the April 4 issue was sent to me by a friend. In your conclusion, you admitted not knowing half of the good electronic hoax stories in the world. Conversely, you can't know all that is true.

Your reference to Nikola Tesla reminded me of a letter once received from a technician who was skeptical of Tesla's claims of having produced "electrical movements not only approximating, but, as shown in many comparative tests and measurements, actually surpassing those of lightning discharges." The skeptic informed me that lightning discharges reach distances measured in miles. No human, he wrote, could produce man-made lightning that long.

When quoted out of context, Tesla's words appear farfetched. The writer's skepticism is understandable. However, when I asked the skeptic if he had ever analyzed Tesla's work or read papers of those who did, his reply was negative. Experts on lightning have shown that thunderclouds vary in coulombs from 12 to 600. When researchers James and Kenneth Corum analyzed Tesla's experiments at Colorado, they determined Tesla's machine to have achieved 260 coulombs. Consequently, the two researchers concluded that Tesla's claim "was no overstatement."

Your skepticism regarding Tesla's claim of wireless power, megavolt sparks, and oscillators producing 10 million horsepower also is understandable. When read out of context, the claims appear so extreme as to warrant ridicule. But, I must ask you the same question that I put to the above mentioned skeptic. There is no need to respond, I know the answer.

Although the mysteries of Tesla's work have not been completely resolved, there exists today a better understanding of what Nikola Tesla did and what he might have accomplished. Tesla spent a year on the Colorado plateau in developing a magnifier that was capable of 100-ft. discharges. He calculated that his machine had achieved 20 million volts at 1100 RF amperes. Armed with new knowledge, he established a plant on Long Island (N.Y.) fully intent on achieving the results to which you refer as a hoax.

A hoax is defined as a trick or a fraud. However, Tesla believed in his calculations and his ability to achieve the desired results. One might accuse Tesla of miscalculation or overstatement, but that would not constitute a hoax.

If you have any interest in Tesla's work, you might find some satisfaction in reading Leland I. Anderson's *Nikola Tesla On His Work With Alternating Currents* (distributed by Twenty First Century Books, P.O. Box 2001, Breckenridge, CO 80424.)

HARRY GOLDMAN
Tesla Coil Builders Association
Queensbury, N.Y.

The energy in a capacitive discharge is $1/2(CV^2)$. *The amount of coulombs is significant, but I doubt if Mr. Tesla's voltages were as large as those found in nature. I will certainly agree that Tesla's achievements were impressive, amazing, and great engineering.—RAP*

Dear Sir:

I'd first like to say how much we all enjoyed your Pease Porridge in the April 4 issue. We have even had people asking for gold-plated mains fuses in the belief that putting a micron or two of gold in the path of the 240-V, 50-Hz mains supply will some how improve the sound of hi-fi... I've considered writing to them suggesting that they ensure that they only receive electricity through underground cables, since cables on pylons might pick up RF.

However, on a more serious subject, I have to take issue with you over ISO 9000. There are so many misleading statements published about this thing that it isn't surprising that even people like you repeat them. However:

ISO 9000 was not an invention of European bureaucrats. It was actually devised by the British Government during World War II to reduce the vast numbers of inspection systems, contract systems, etc., which were making it hard to ensure that we had the right tools to upset Hitler. After the war, it developed (slowly) into BS5750, the BS standing for British Standard rather than male bovine excreta. BS5750 became ISO 9000 as a result of ISO activity—and ISO is an international body on which virtually every major country is represented, including the U.S.

North Americans tend to forget, or perhaps underestimate, the importance of the fact that in Europe, we have a variety of languages and cultures, and this includes different ways of doing business and different attitudes to the customer. The European Commission has promoted ISO 9000 as a way of removing some of the confusion, just as BS5750 was intended to do during wartime. It means that now, when I try to assess whether (say) an Italian or German supplier has the systems in place to resolve potential quality problems and to give my company what it wants, I have at least some framework to look at with which I have some acquaintance, and that with my limited Italian and German, I can still have a sensible conversation with the supplier. I have to say that from my experience, ISO 9000 is working for us.

It's a means of setting up a quality system with all the necessary parts—calibration, monitoring production, assessing cost of quality, handling customer complaints, etc. It ensures that all essential areas are covered, more or less in the same sort of way. It says nothing about what the quality of a product produced by a company is. This is just like accountancy, which has standard rules for measuring money. You might have a perfect accounting department and still be going down the pan owing to a severe negative profitability situation. Equally, you might have a perfectly run QA system and make rubbish. However, in both cases, you and people who depend on you will know exactly how bad things are and probably be able to identify some sensible actions.

Many small companies get started and run for years without ever knowing that there are some things they should be doing—keeping records of product introductions and changes, calibrating equipment, etc. All is fine until the day something goes very wrong and someone is in a position to sue them into the ground. For these people, ISO 9000 is a relatively cheap insurance policy. For large companies, with their own hierarchical management systems, this is less of a problem.

If there is a hoax, it is probably promoted by the people who seem to regard certification to ISO 9000 as some sort of quality achievement. It isn't. It was never meant to be. It is an organizational achievement.

My company makes safety-critical products—fuses—lots and lots of them. In Europe, the quality achievement is shown by those arcane symbols—BSI Kitemark, VDE triangle logo, and so on. The bodies that do the testing and the certification believe that our registration to ISO 9000 is evidence that we have a quality system strong enough to ensure that deviations from our quality norm will be quickly detected and made right. It is the combination of ISO 9000 and product approval that is the real measure of quality achievement.

For this reason, the real European Bureaucracy bit is the CE mark. This mark attached to a product is a statement that the manufacturer complies with every quality and performance requirement relevant to product safety, and can prove it. It corresponds, very roughly, with UL listing.

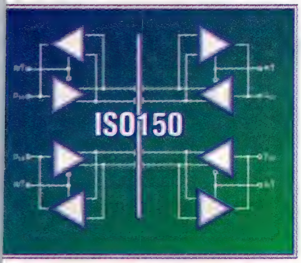
MARTIN BACON
Cooper Bussman
Somerset, England

If ISO 9000 is really like you say it is, then all of the confusion and misrepresentation and bragging we see is even more disgusting. I have yet to meet anybody that's in charge of im-

RR - BROWN®
BB

UPDATE

ew Isolated Bi-Directional Digital oupler is Better than Optocouplers



Circle Reader Service No. 281

0150 was designed to replace tocouplers— it uses high voltage pacitors instead of an LED/photodiode mbination to transmit signals across e isolation barrier. (Optocouplers quire large current pulses to drive the D, causing noise spikes on the power pply line.) **ISO150**'s combination of w power, high speed, and low cost lves many design limitations inherent optocouplers—it's a reliable and cost fective alternative! And, **ISO150** is very sy to use—no external components e required.

ISO150 is an ultra high-speed capacitively coupled digital device that delivers high isolation with very low power consumption. It has two, bi-directional channels—each channel can be configured independently to transmit or receive signals across the isolation barrier. Use it for a variety of applications including digital isolation for A/D and D/A conversion, multiplexed data transmission, computer-to-peripheral interfaces, I/O port isolation in instruments, power conversion, and isolated data acquisition systems.

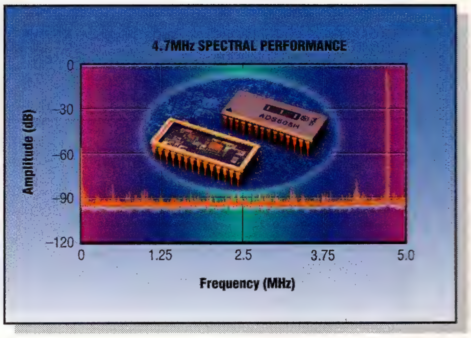
ISO150 key specifications:

Data rate	80MBaud typ
Power consumption per channel	25mW max
Isolated rated continuous	±1500Vrms
Isolated partial discharge (tested)	12400Vrms
Isolated 1 minute stress (tested)	4000Vrms
Creepage distance	16.5mm

ISO150 is priced from $6.80 in 1000s.

ynamic 12-Bit, 10MSPS A/D

S605 is a 12-bit mpling A/D that ovides the highest quist performance in product category at e lowest price. It's a mplete device with ideband track/hold, -bit quantizer, timing rcuitry, and low drift ternal reference all in economical 28-pin P. **ADS605** is an cellent choice for emanding imaging, mmunications, and test/ easurement applications.



Circle Reader Service No. 282

uaranteed Nyquist Success

oth DC and dynamic AC specifications e guaranteed to Nyquist rate. The ideband track/hold, with its 32MHz ll-power bandwidth, gives designers utstanding spurious-free dynamic nge, and SINAD. **ADS605** also accepts ngle-ended inputs, eliminating the dditional time, parts, and power eeded when using competitive evices with differential inputs. Power ssipation is also very low for a high erformance sampling A/D.

An optimum layout, fully assembled demo board is available to facilitate fast, accurate evaluation.

ADS605 key specifications:

Sampling rate	10MSPS
SFDR	–78dBc
DNL	0.5LSB
SNR	66dB
Power dissipation	1.4W
Resolution	12-Bit

ADS605 is priced from $125 in 1000s.

Circle Reader Service No. 283

Precision Instrumentation Amp Consumes Only 350μA

INA118 is a precision instrumentation amplifer ideal for battery powered systems and other low power applications. It's a power miser—**INA118** operates with power supplies as low as ±1.35V, or single supply operation to 2.7V. Quiescent current is only 350μA. Internal input protection withstands up to ±40V without damage.

A single external resistor sets any gain from 1 to 10,000, and current-feedback input circuitry provides wide bandwidth, even at high gain (70kHz at G=100). Use the **INA118** for portable instruments, thermocouple amplification, medical instrumentation, and general purpose data acquisition designs. It's available in space-saving 8-pin DIP, SO-8 surface mount, and die form.

INA118 key specifications:

Offset voltage	50μV max
Drift	0.5μV/°C max
Input bias current	5nA max
CMR	110dB min
Power supply	±1.35V to ±18V
Quiescent current	350μA

INA118 is priced from $3.25 in 1000s.

And the Winners Are...

The ***ADS Family Design Contest*** was a big success—it generated more than 80 great circuit ideas from our smart customers. Innovative ideas ranged from a circuit that powers, controls, and reads output data over a coax line to an anti-stress computer keyboard alarm circuit. Five inventive designers won $2000 gift certificates for computer products. We thank and applaud everyone who entered!

GREAT IDEAS FROM OUR SMART CUSTOMERS

The Winners —

- *Dr. Ing. Hans Joachim Goetz,* Nuernberg, Germany
- *W. van Hoek,* Terneuzen, The Netherlands
- *Narottan Patel,* San Jose, California
- *Alexander Petnuinas,* Dearborn, Michigan
- *Daniel Steiner,* Bern, Switzerland

Keep designing-in the ***ADS Family***—bit for bit the best A/Ds ever!
Look for more contests in future issues of Update!

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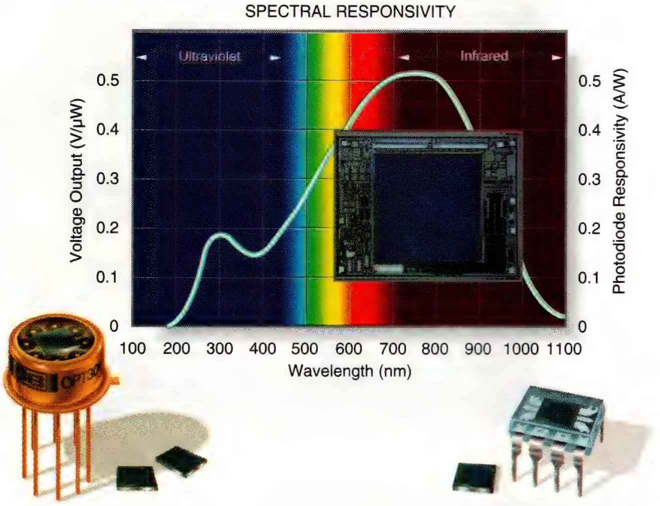


Circle Reader Service No. 284

New

Photodiode ICs Simplify Instrumentatio and Scanning Applications

OPT202, **OPT209**, and **OPT301** are three new additions to our rapidly expanding line of low cost, high performance optoelectronic products for precision instrumentation, scanning, and sensing applications. These new ICs integrate a large 0.09" x 0.09" photodiode and precision FET-input transimpedance amplifier on a single chip. Photodiode current is converted to an output voltage proportional to the light's intensity.

All devices share common features: a large, sensitive photodiode; a 1MΩ feedback resistor; high responsivity, 0.45A/W; low dark errors, and a wide ±2.25 to ±18V supply range.

- **OPT209** provides excellent performance for general purpose applications. Bandwidth is 16kHz.
- **OPT202** extends bandwidth to 50 and is ideal for pulsed-light applications such as barcode scanners. **OPT202** and **OPT209** ar packaged in 8-pin clear plastic DIF
- **OPT301** provides improved ultraviolet response—an excellent choice for use spectrophotometers and fluorescence detectors. Its hermetic TO-99 package protects against hazardous environme

OPT202 is priced from $5.25 in 100 **OPT209** from $4.25; and **OPT301** from $9.55.

Precision FET Op Amp Features Ultralow 6nV/√Hz Noise

OPA124 is our new, precision op amp that combines low prices with outstanding AC and DC performance for critical instrumentation, data acquisition, and optoelectronic applications. Its *low* bias current, *low* noise, *low* voltage offset, *low* drift mean the highest performance available in a surface mount package—superior even to BiFET and CMOS amps. And, **OPA124**'s patented dielectric isolation (***Difet***®) processing and unique cascode design minimize input errors and simplify filtering requirements.

2 packages, 3 grades

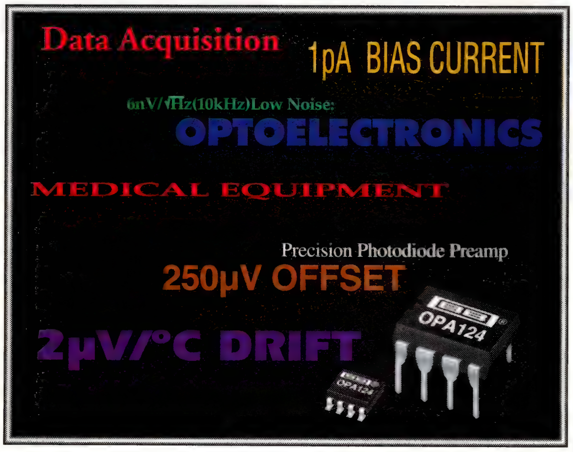
OPA124 is available in 8-pin plasic DIP and surface mount packages. It also comes in three performance grades. Our highest grade specs in SOIC can't be beat by any competitor! You pick the perfect performance grade for your specific application.

OPA124 key specifications:

Noise(10kHz)	6nV/√Hz
Input bias current	1pA max
Input voltage offset	250µV max
Offset average drift	2µV/°C max
CMR	100dB min
Open-loop gain	120dB min

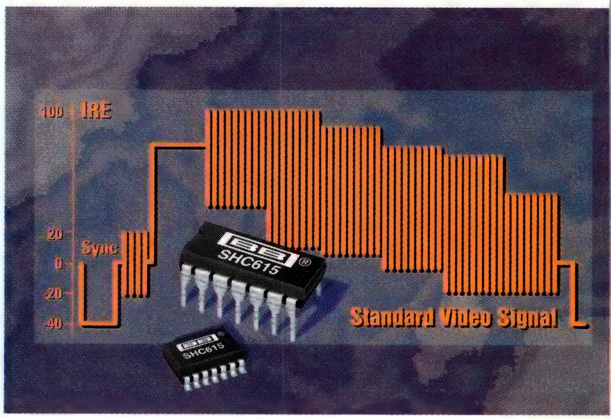
OPA124 is priced from $3.12 (lowest grade, in 1000s).

Circle Reader Service No. 285



New

DC Restoration Circuit for Video



Circle Reader Service No. 286

SHC615 is a unique DC restoration device ideal for high speed, precision applications. Designed to stabilize the performance of RF signals, **SHC615** is also useful for other applications such as a fast phase comparator, a synchronous demodulator in PLL circuits, or a RF pulse code mod/demod.

Sampling Uses

SHC615 can also be configured as a sampling comparator—with high impedance differential inputs, current source output, and a fast switching stage with TTL/CMOS compatibility. **SHC615** can also be used as a high speed peak detector and as a double sampling correlator that improves the SNR of CCD-generated signals.

In a single 14-pin plastic DIP or SOI package, **SHC615** is specified over th extended industrial temperature rang of –40°C/+85°C.

SHC615 key specifications:

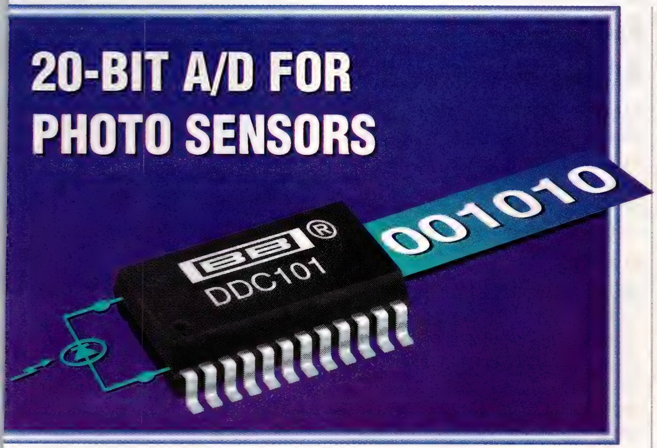
Bandwidth	280
Propagation delay	2
Slew rate	1700
Noise	4nV/
Power dissipation	600mW

SHC615 is priced from $7.95 in 100s

BURR - BROWN® FAX*LINE*
800-548-6132

ISO9001 CERTIFIED

For fast product info, call **1-800-548-6132** or fax **602-741-3895**.



Circle Reader Service No. 287

w 20-Bit A/D for Photodiodes d Other Low-Level Current Signals

101 is a 20-bit, current input A/D erter designed for direct connection otodiodes and other low level current ut devices. It replaces an amplifier t, programmable-gain amplifier, and resolution A/D converter—all on a e, monolithic chip. **DDC101** is an vative solution for many precision umentation and process control cations including direct photosensor zation, medical and chemical zers, and infrared pyrometry.

vative Patented Architecture

101's patented delta modulation ogy was specifically designed for sion quantization of extremely low sensor outputs. Using digital ration, oversampling, correlated le sampling, and digital filters, this e improves noise and linearity as the level decreases. Or, *as the input al gets smaller and smaller, the* **101** *gets better and better*—with an input signal of 0.1% full scale the maximum linearity error is only 0.0003% FSR! Its conversion rate is up to 15kHz.

DDC101's advantages over delta sigma or integrating converters include much higher speed, better linearity and noise for small signals, direct low level current input, direct connection to photosensors, and no digital filter latency. Errors, cost, and board space are greatly reduced.

A demonstration board is available ($350) for fast, accurate evaluation and prototyping.

DDC101 key specifications:

Resolution	20-Bit
Noise	0.9ppm, rms
Conversion rate	up to 15kHz
Accuracy	3ppm of FSR, rms
Power dissipation	170mW
Digital error correction	CDS

DDC101 is priced from $22.95 in 1000s.

20-Bit Digital Audio A/D System Delivers 108dB Dynamic Range

Our new **PCM1760** A/D converter, together with its matched **DF1760** digital filter, gives digital audio and multimedia designers the best combination of analog and digital performance ever available for under $30!

Better Than 1-Bit!

The "1760" system is the first to feature our proprietary "multi-bit enhanced noise-shaping" circuitry. This unique, innovative approach delivers wider dynamic range and lower noise than 1-bit designs while avoiding loop oscillation, jitter sensitivity, and process speed problems common to older architectures. The design achieves superior performance from our small, inexpensive monolithic circuits previously only available in larger, more expensive modules and hybrids.

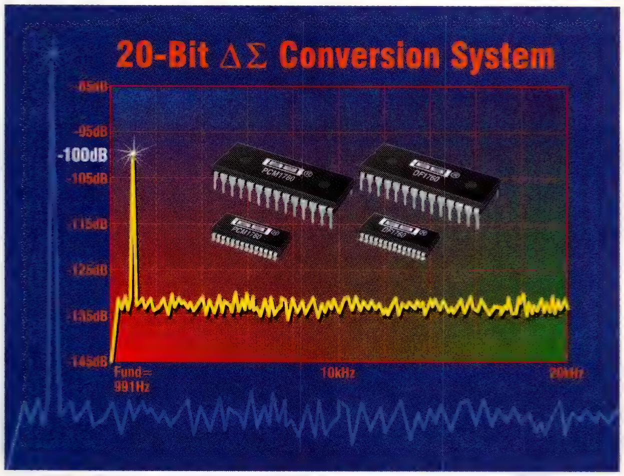
PCM1760 operates from ±5V supplies, **DF1760** from a single 5V supply. Both are specified for the 0/+70°C temp range. **PCM1760** and **DF1760** are available in 28-pin DIP and 28-lead SOIC.

PCM/DF1760 key specifications:

Resolution	20-bit
Dynamic range	108dB
THD+N	–92dB
SNR	110dB
Channel separation	98dB
Oversampling	64X
Noise	1.6ppm, rms
Conversion rate	up to 15kHz
Accuracy	3ppm of FSR, rms
Power dissipation	170mW
Digital error correction	CDS

PCM1760 starts at $14.37 in 1000s, **DF1760** from $15.52.

Circle Reader Service No. 289



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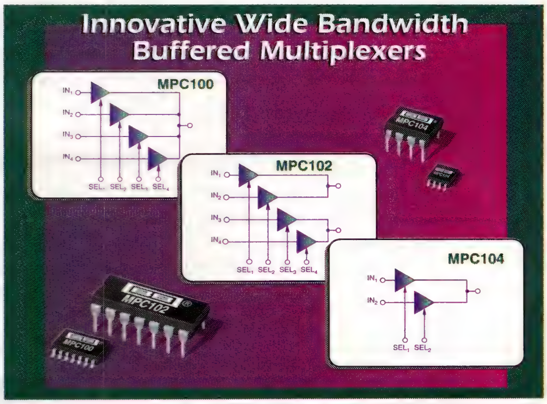

New Multiplexer Family is Ideal For Video, RF Designs

Three new wideband, buffered multiplexers give customers a range of analog signal routing solutions for their video, radar, RF, and data acquisition applications.

- **MPC100** is a 4 X 1 multiplexer.
- **MPC102** is a dual 2 X 1 multiplexer.
- **MPC104** is a single 2 X 1 multiplexer.

This family of multiplexers feature exceptionally high output-to-input isolation, 210MHz bandwidth, and slewing ≥ 500V/μs.

Differential gain and phase errors are as low as 0.02% and 0.01°, respectively. All parts offer very low crosstalk, low switching transients and low quiescent current. They operate from ±5V supplies with –40°C/+85°C specified temperature ranges.

MPC100 and **MPC102** are offered in 14-pin DIP and SO packages; **MPC104** in an 8-pin DIP and SO. Dice are available. **MPC100** pricing starts at $7.41; **MPC102** at $7.41; **MPC104**, $4.94 in 100s.

For fast product info, call **1-800-548-6132** or fax **602-741-3895.**

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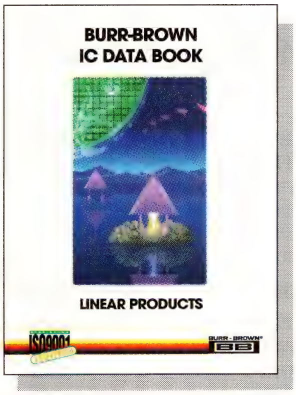
UPDAT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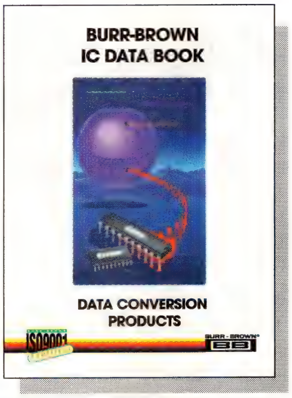
IC DATA BOOK

LINEAR PRODUCTS


BURR-BROWN
IC DATA BOOK

DATA CONVERSION
PRODUCTS

Circle Reader Service No. 290

Product Info—

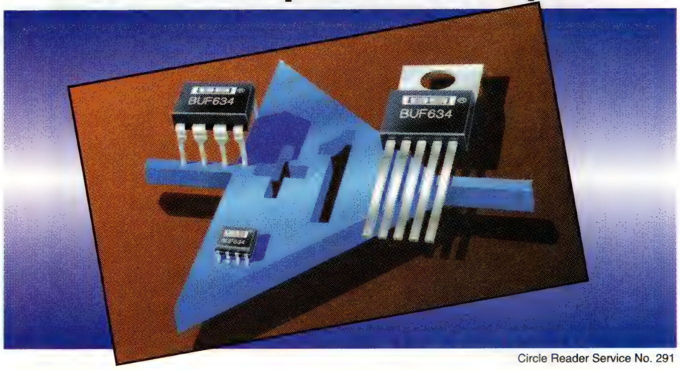
Two New Integrated Circuits Databooks

Our two new *Integrated Circuits Data Books* give designers more than 60 new high performance linear and mixed signal solutions. Both the *Linear Products* and the *Data Conversion Products* data books include complete product descriptions and specifications, applications tips, performance graphs, and ordering information.

The *Linear Products Data Book* profiles op amps, instrumentation amps, isolation products, references, and regulators. The *Data Conversion Products Data Book* profiles A/Ds and D/As, data acquisition components, sample/hold amps, VFCs, multiplexers and more.

FREE from local sales representative or call **1-800-548-6132**.

250mA Buffer Amp Slews 2000V/μs



Circle Reader Service No. 291

BUF634 is a high speed, unity-gain buffer amplifier that delivers 250mA output and 2000V/μs slew rate—all in a tiny SO-8 package. Its low price, high performance, rugged monolithic design, and ease of use make **BUF634** ideal for general purpose driver applications including valves, solenoids, video, and even headphones.

Ups Output, Not Errors

BUF634 can be connected inside the feedback loop of most op amps—increasing output current without introducing errors. Its bandwidth can be pin-programmed for 30MHz with 1.5mA quiescent current or boosted to 180MHz with 15mA quiescent current.

BUF634 operates from a wide supply range, and its internal current limit and thermal shutdown protect against load faults and short-circuits.

BUF634 comes in an SO-8 surface mount package, an 8-pin plastic DIP, a 5-pin TO-220, and in die form. The SO-8 package is the industry's smallest 250mA buffer, while the TO-220 tab-mounted power package provides the best thermal performance for heavy duty applications.

BUF634 key specifications:

Output current 250mA
Slew rate 2000V/μs
Bandwidth ....30MHz to 180MHz
Power supply ....±2.25V to ±18V
BUF634 is priced from $2.60 in 1000s.

New 16-Bit D/A For Industrial Applications

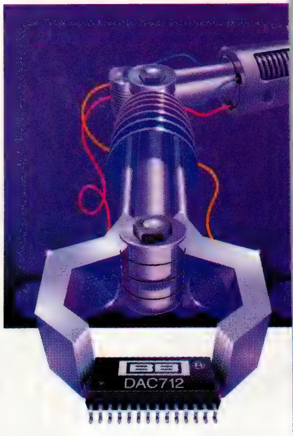
DAC712 is a new 16-bit D/A designed and specified for industrial applications. It offers important advantages to customers involved with ATE equipment, analog I/O boards, robotics, process controllers, and similar designs.

Easy To Use

DAC712 features a fast, 16-bit parallel, double-buffered interface for direct connection to industrial buses. Gain and offset adjust make autocalibration easy with external D/As. It operates over a power supply range of ±12V to ±15V. The output swings ±10V on ±12V supplies.

Beats the Competition

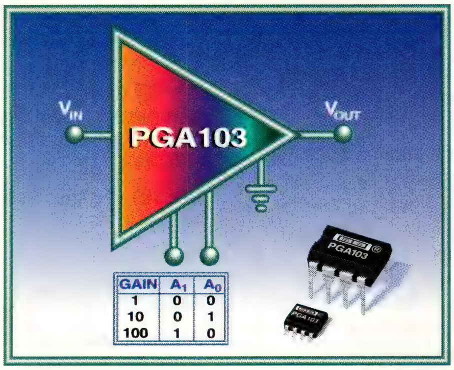
DAC712 beats the competion in price, power, and package size. It's packaged in a 28-pin, "skinny" 0.3" DIP—half the size of our competition! Power dissipation is a low 600mW, and prices have been cut, too! Specified over the extended industrial temp range, it's available in a 28-lead SOIC package.



Circle Reader Service No

DAC712 key specifications:

Resolution 16-
Settling time.........................10μs (m
INL............................13 bits and 14 b
Power supply....................±12V to ±1
Power dissipation ....600mW m
Voltage output................................±1
DAC712 is priced from $13.00 in 100



GAIN	A_1	A_0
1	0	0
10	0	1
100	1	0

Circle Reader Service No. 29

New Low Cost, Easy-To-Use, 8-Pin Programmable Gain Amplifier

PGA103 lets you digitally select gains of 1, 10, and 100 using just two TTL– or CMOS-compatible control lines. This tiny 8-pin amplifier offers a simple way to change circuit gains, cheaper than in-house designs, and easier to use than existing PGAs. It's an excellent choice for systems handling wide dynamic range signals, including medical, analytical, and scientific instrumentation and data acquisition systems.

Fast and Accurate

PGA103 is fast—for multiplexed systems. Its low gain error eliminates expensive precision resistors require in homemade PGA circuits. Compact 8-pin plastic DIP and SOIC packages save board space without sacrificing function or performance.

PGA103 key specifications:

Bandwidth ....250kHz (G=100
Settling time
...................2.5μs to 0.01% (G=1, 10
Gain error............±0.05% max (G=10
Gains 1, 10, 100V/
Quiescent current 2.6m
PGA103 is priced from $3.30 in 1000

PEASE PORRIDGE

plementing ISO 9000 who knows any facts, who knows what really is supposed to happen. The implementation of ISO 9000 is where you don't see quality.—RAP

Dear Bob:

Enjoyed reading your article on "Hoax Stuff." However, I was surprised that you didn't mention the Master of all electronic hoaxers, Hugo Gernsback. I am sure you remember him as the publisher of *Popular Electronics* magazine (or was it *Modern Electronics*)? My memory is starting to fade. Anyway, come every April you were sure to find one of his electronic hoaxes in his magazine, complete with all the details.

Of course, when I was much younger (in the early 60s), I didn't know this and as a young and enthusiastic electronic hobbyist, I would build anything for which I could find the parts. One of his articles described the construction of an "anti-electron generator" or something close to that (remember, my memory). The purpose of the anti-electron generator was to do just the opposite of what you would expect a normal generator to do.

For instance, if you plugged a soldering iron into the generator, instead of the tip becoming hot, frost formed. I think you get the idea.

Also, being an amateur photographer, I was more interested in the lamp. When you plugged in an ordinary lamp, instead of light (you guessed it) it took away all of the light in the room and made it dark. What a fantastic invention! I couldn't wait to build my very own. There it was, all the details, schematic, parts lists, photos, and text.

It wasn't until I collected half the parts that I bothered to read the rest of the article. There was one sentence at the end that I didn't understand at first, "...and the circuit only works well on April 1st." I was hoaxed. I was mad, but now I'm glad.

No school could have taught me the lesson I learned from this experience. For the rest of my life, I would treat all circuits (including my own), and all other claims as hoaxes until proven otherwise. Thank you Mr. Gernsback, wherever you are.

A few years ago, I bought a book from Gernsback Publishing, which had a few dozen of his hoaxes, unfortunately not the one above. I was going to send you the book, but I can't find it right now. In the meantime, I thought you might enjoy my story.

GARY C. FIELDS
VP Engineering
Merge Technology Group Inc.
Napa, Calif.

Ah, yes, those "macro-wave ovens" that cool their contents, always have some appeal!!—RAP

Dear Bob:

I enjoyed your article on hoaxes, and would like to add a few I've seen or heard of.

Several years ago I saw an ad for an indoor TV antenna that looked like a combination of rabbit ears and a miniature satellite dish. There were several paragraphs of impressive fine print. The unique thing about this ad was it contained no lies at all. It was guaranteed not to incur any cable or satellite fees because it was not designed to pick up any cable or satellite channels. It had the wonderful ability to intercept TV signals right out of the air! They didn't even claim a technological breakthrough. The claim was that this was a "Marketing Breakthrough."

About 25 years ago, there was an article in one of the ham magazines about a "buried antenna" that was said to propagate "ground waves."

A thought on audio specs; if people can get away with making such extravagant claims for a piece of wire, I wonder how many of the specifications for more complex components really relate to differences you hear. Your comments on people with "Golden Ears" reminds me of the "Emperor's New Clothes."

In 1978, an "inventor" named Rory Johnson, of Elgin, Ill., received lots of media attention in the Chicago area for his "Magnetron" car engine, which weighed about 500 pounds, produced 525 hp, and would run for 100,000 miles on a self-contained supply of gallium (a well-known donor source for electricity) and deuterium. He claimed a laser beam caused a fusion reaction between the two elements. He demonstrated a car with the engine idling, but no one saw the car actually run on the engine due to "safety reasons." Unfortunately, this was not just a hoax, but a fraud, as investors lost hundreds of thousands of dollars. (*Daily Courier News*, Elgin, Ill., Aug. 12, 1977 and Dec. 22, 1978)

KENNETH LUNDGREN
Bloomingdale, Ill.

Yes—some hoaxes only cost you $5 or $10—and others can cost the gullible a whole lot more. People who want something for nothing...—RAP

Dear RAP Chap:

Re Hoaxes: My favorite is the "Little Jiffy Fuse Blower" published in *Electronics* (?) before (?) 1953.

Here, a heavy-duty push-button switch was paralleled with an Amphenol chassis-mounting ac line plug in a neat little minibox (about 2-in. cube). The device title is neatly lettered on the box. The builder is instructed to leave the device loose and unguarded on the desk. The device will disappear and soon thereafter the lights will go out in a section of the office. A shamefaced new believer soon sneaks the device back. The author was exactly right, but he didn't mention the switch needs replacing after four or five episodes.

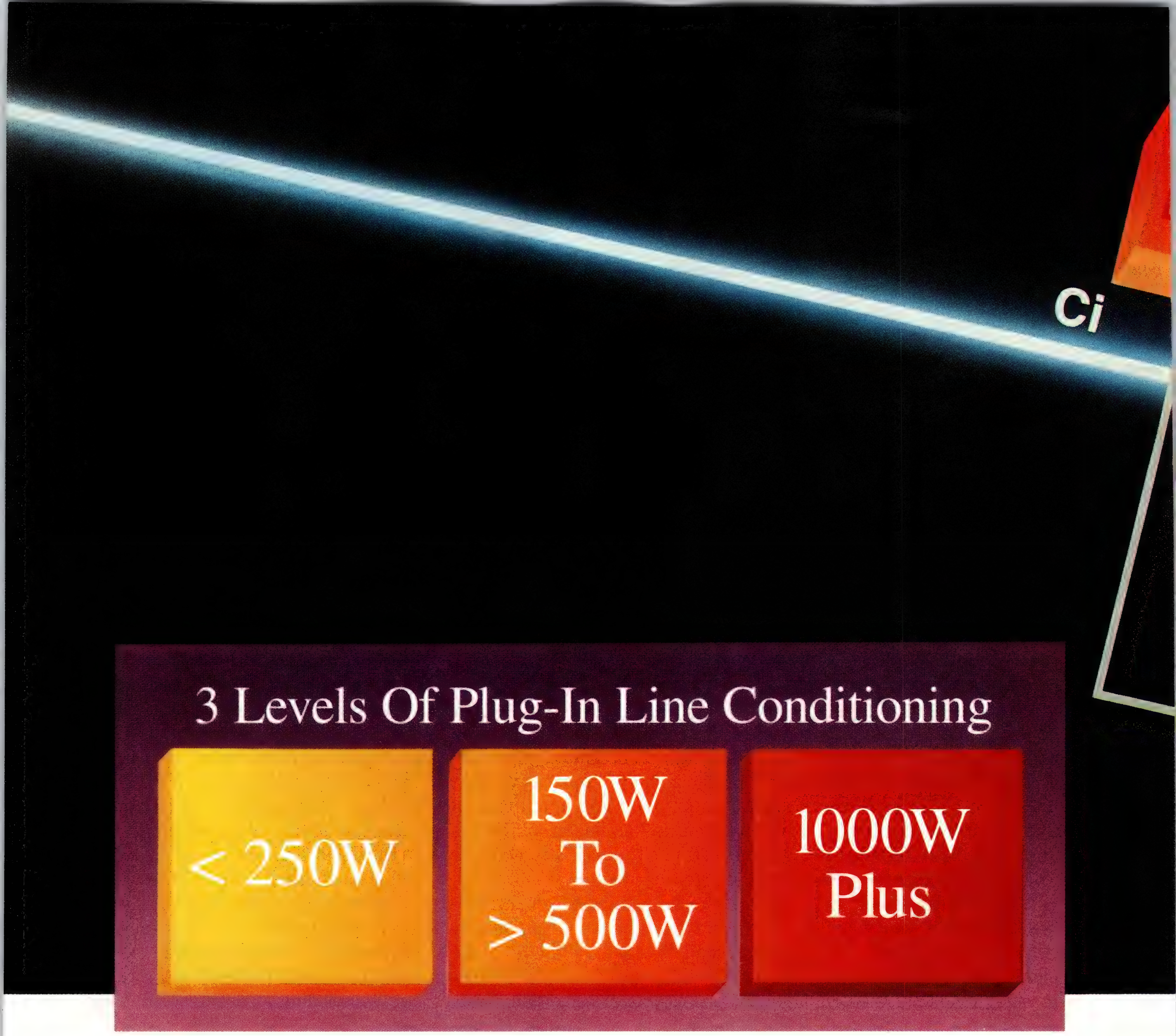
Our local "911" bureaucrats with Postal Service help have renumbered and rezipped our entire road. This falls somewhere between an April fool joke, a hoax, and a fraud. (Some time, figure out change-of-address costs. Of course you shouldn't count the fine for having the wrong address on your driver's license.)

DAVE GEISER
New Hartford, N.Y.

Yes, several people sent in the "Fuse Blower." In our lab, a specialty was to give a guy a National Semi calculator, that would smoke and burn and explode when switched on!—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090


Ci
3 Levels Of Plug-In Line Conditioning
< 250W
150W To > 500W
1000W Plus

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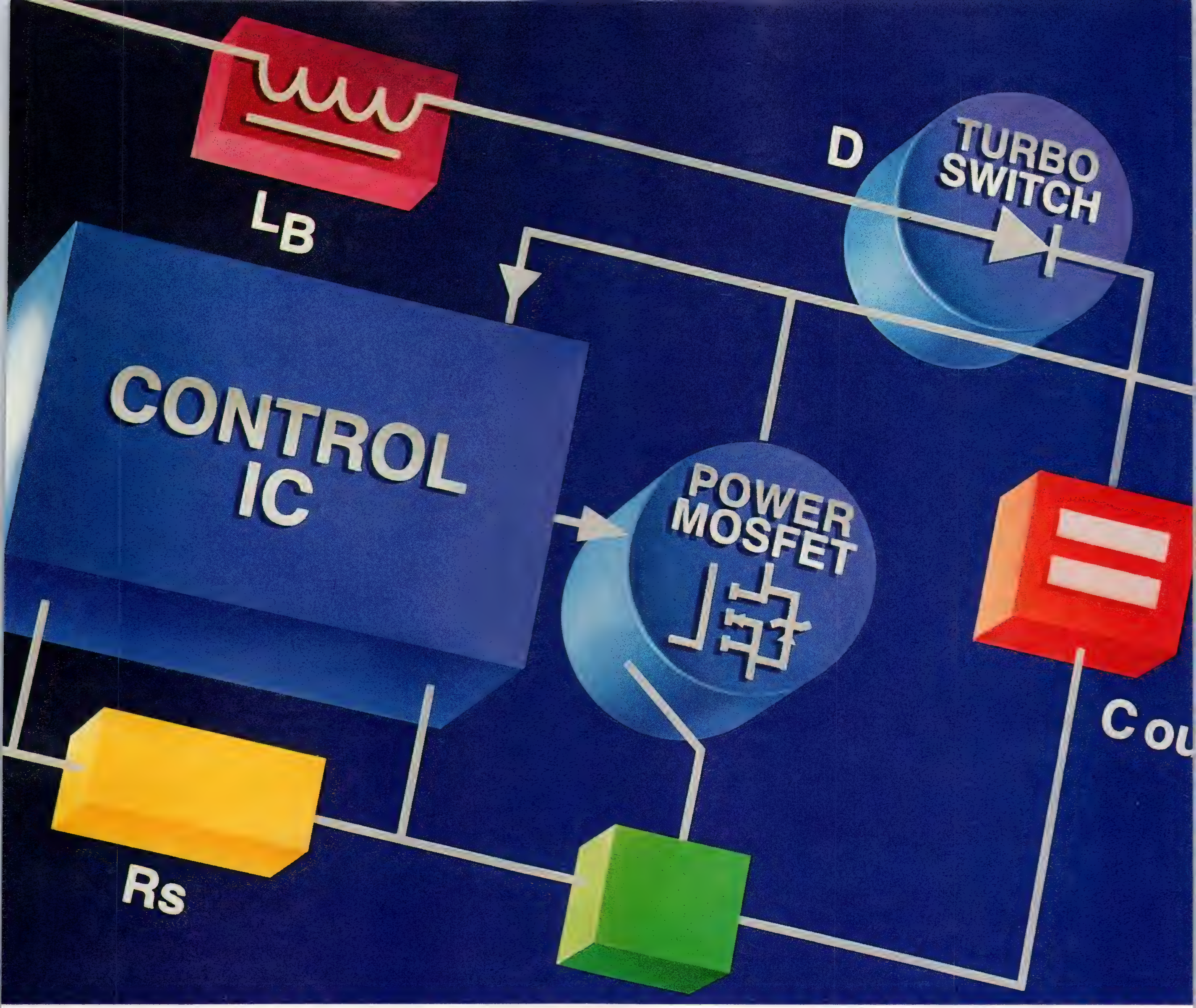

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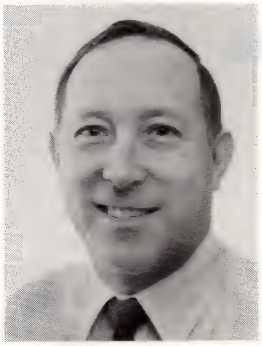
PLUGGING INTO PCMCIA

PCMCIA SCSI HOST ADAPTERS

BILL CALDWELL, QLOGIC CORP.

With the growing popularity of notebook and subnotebook computers, PCMCIA is becoming the industry standard for incorporating enhancements to these systems. The low-power requirement and the limited space available for adding options to notebook computers make the credit-card-sized PCMCIA card a practical solution.

Originally intended as a means to add memory devices to notebook computers, the PCMCIA specification was revised to include other devices. The specification now supports various I/O cards, as well as the memory cards. The growing list includes RAM, EEPROM, flash memory, fax-modems, rotating disk drives, LAN, sound, and SCSI cards.



Adding a PCMCIA SCSI card to a notebook provides the same options as adding a SCSI host adapter to a desktop computer. It also offers some features not available on a desktop computer that uses traditional ISA-based host adapters. A PCMCIA SCSI card provides a method of connecting nearly any SCSI device to a notebook computer. This includes disk, tape, and CD-ROM drives; scanners; and SCSI printers. The small size of the PCMCIA SCSI card doesn't mean that its performance is less than would be expected from a SCSI host adapter in a desktop computer. In fact, with today's 486-class notebook computers, PCMCIA SCSI host adapters can outperform ISA SCSI host adapters using master-mode DMA capabilities.

A feature of the PCMCIA SCSI card unavailable with desktop computers is the ability to "hot swap" PCMCIA cards. In other words, the PCMCIA card can be inserted or removed without powering down or rebooting the computer. In addition, some PCMCIA SCSI cards, such as the card offered by QLogic, can automatically configure the SCSI devices. This allows SCSI devices to be added or removed without having to reboot the computer or making any software modifications. For proper operation, the card and its associated software drivers must be compliant with the PCMCIA hardware and software specification.

While PCMCIA is maturing as a standard, some issues still must be addressed. One of those issues confronting computer manufacturers concerns the interrupt levels available for use by PCMCIA cards. There's no standard number of interrupts available for configuring PCMCIA cards, which can lead to problems when trying to configure a card on some computers.

Designers must handle the resource allocation when multiple PCMCIA cards from different manufacturers are installed in the same system. Due to a lack of sufficient rules to determine resource conflicts, sometimes different cards are allocated the same I/O or memory address, causing the system to operate erratically. This problem can be avoided by manually assigning the necessary addresses during the installation process.

Another issue is the inability to boot from a PCMCIA I/O card. The PCMCIA specification stipulates that a subset of the standard ATA interface must be implemented to support small hard-disk drives in a bootable fashion. To fully recognize the potential offered by SCSI to support various bootable devices, such as RAID arrays and large hard-disk, optical, and tape drives, system BIOS manufacturers must incorporate the ability to recognize and execute from the BIOS on the PCMCIA card.

While this sounds like a simple task, because of the different chips available to generate the PCMCIA socket interface, each notebook computer manufacturer must customize the system BIOS to configure the PCMCIA socket, then identify and configure the bootable PCMCIA adapter. Once this is done, the actual PCMCIA card BIOS must be executed, which would in turn automatically configure the attached SCSI devices and boot from the selected device. Although this technique can be implemented several ways, the preferred method requires a subset of the card and that socket services be resident in the system BIOS.

Before the PCMCIA bus can realize it's full potential and support bootable SCSI devices, these unresolved issues must be dealt with. The PCMCIA committee has formed a task force to generate a proposal. However, it doesn't look like there's a sufficient amount of time to adopt the proposal into the next major release of the PCMCIA specification. In the meantime, the industry will see a variety of non-standard solutions for these issues.

For more information on the PCMCIA SCSI specification, or any other issue involving PCMCIA, call the standards organization at (408) 720-0107.

Scaling I/O Bandwidth With Multiprocessors

Scalability lets the application determine the processing power.

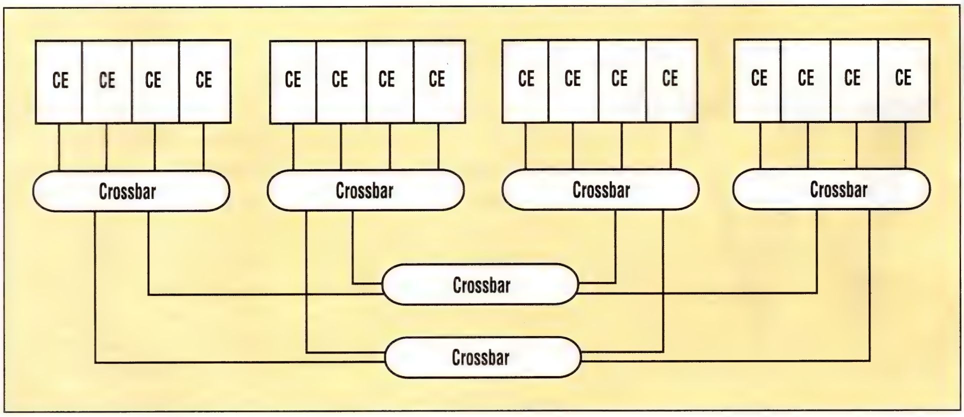
BY BARRY ISENSTEIN

Mercury Computer Systems Inc., 199 Riverneck Rd., Chelmsford, MA 01824; (508) 256-1300.

Though the term "one size fits all" has proven to be a misnomer over the course of time, computer designers seldom have the luxury of time or resources to create a unique solution for every application. Products, technologies, organizations, and applications are changing at an increasingly faster rate. To be economically viable, most designs leverage existing solutions on-the-fly to address new situations. Key to that leverage is the notion of scalability, meaning that the solution should work as well in as many different versions of itself as possible.

The benefits of I/O scalability for real-time multicomputing include: the same system definition can span many platforms, from one board to multiple interconnected chassis; scalable solutions can be developed as smaller, less expensive systems that are expanded later; and application design risk is reduced because a scalable architecture lets users adapt the system as requirements change or if they need to upgrade their systems.

Reviewing the limitations of non-scalable I/O solutions, such as the bus, makes it easier to appreciate the benefits of scalability. Buses inherently trade performance for size and efficiency. Increasing the speed of a bus bolsters its width, frequency, and cost, while decreasing its length and efficiency for small transfers. Users who attach fewer than the maximum number of processors a bus can handle may be wasting money and space. Users looking to add more than the maximum number might need to redesign using a different bus. In other words, the I/O cost per processor for a non-scalable solution, such as a bus, drops as more processors are added, up to it's maximum allowable number. Once the maximum is surpassed, cost then increases. In a scalable solution, the I/O cost per processor remains the same.



1. Redundant lines supply separate paths for real-time and system traffic. The scalability is integrated because the CEs can address a particular I/O profile or a range of I/O profiles.

An alternative to buses are point-to-point interconnects implemented as ASICs, called crossbars. Although crossbars aren't new, they have yet to catch on as a serious substitute to buses. Case in point: as of yet, there are no crossbar-based interlink standards similar to bus standards. An architecture based on crossbars also must provide backward compatibility to established bus architectures, such as the VMEbus.

Different applications and different sizes of the same application have unique I/O profiles. The goal of a scalable interlink is to accommodate many I/O profiles by connecting together the same set of inexpensive parts while maintaining a standard interface to the outside world.

An I/O profile dictates what the interlink must do to achieve efficient data transfer. Three issues decide an application's I/O profile—the data type, the overhead, and the data distribution. The data type refers to the nature of the data to be transferred. Overhead is how long it takes to process the transfer request. Data distribution defines the proximity of the data to its processing point.

Two questions that must be answered regarding the data type are: Do the data transfers need to be small or long? And, is there lots of control data being generated relative to external data? If transfers are short, then the most important factor concerning I/O performance may be latency—the amount of setup time needed to handle the shortest piece of data. If the data tends to travel in long, sustained blocks, then throughput is probably more important. It may be okay to take a long time to set up a transfer as long as lots of data can be moved quickly.

Overhead is a function of how much control data the interlink requires in the data stream. The more control data, the higher the latency and the lower the throughput. Removing control blocks implies dedicating re-

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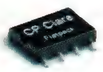
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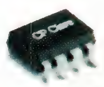
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sources to a processor, such as memory addresses, interrupt lines, and data paths, rather than make the processor either negotiate for them or find out if it "owns" the resource. Control data increases latency by increasing the amount of time it takes to process I/O transfer requests. The more negotiations that occur, the less extensible the architecture. The more scalable the architecture, the more likely it is to supply alternatives to negotiated transfers of data among devices.

Questions related to data distribution include: Is data located near where it's processed? Are there obstacles (i.e., other components) that physically interfere with data transfer? In addition, is all of the data needed for a process located in one place or is it scattered around the system? Badly distributed data can degrade latency performance as well as throughput performance.

Issues of data type, overhead, and distribution often seem to be in contention. The I/O profile of one application should not be compromised at the expense of another's profile. To accomplish that, six rules of scalability should be followed:

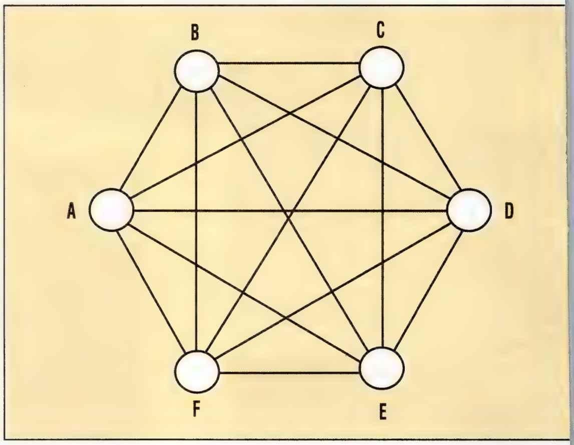
- use building blocks
- separate configuration control from application source code
- provide for deterministic I/O
- provide self-routing data packets
- use transparent buffering of slave transfers to memory from external I/O
- provide I/O that fits a broadcast capability, mailbox interrupts, and shared-memory regions

Defining consistent system building blocks means knowing the functional boundaries that consistently exist within systems. One such boundary occurs between data processing and data transport. The first function is called a compute environment (CE) and the second an environment connector (the crossbar). Note that a CE isn't necessarily a processor because a processor doesn't contain everything needed to manipulate data at a particular location. Whether or not it's implemented on one chip, a CE must supply processor and I/O services. With I/O services, the CE can be configured to match a specific system I/O profile.

System designers must decide what features to include within the I/O services and then optimize them for system-wide implementation. Designers could ensure, for example, that DMA control is implemented so that a complex chain of DMA requests requires no processor overhead. This can be done by working off a link list in memory. The purpose of prepackaging these I/O features with the processor is to allow the CE to be scalable by having it address a particular I/O profile or a range of I/O profiles *(Fig. 1)*.

The opportunity to plug-and-play CE crossbars into various data flows provides the basis for another opportunity—to take deliberate advantage of a design by externally imposing control over the data flow. By implementing configuration control services and deterministic I/O, designers can direct which path particular data will take among several that are available. This can be preferable to relying on bus handshaking for guaranteed delivery of real-time data within a predetermined time. By removing some of the process segmentation burden from the source code, these features can reduce the development complexity.

A configuration-control service implies the existence of programmable paths within the system that can be selected. Thus, routes can be manually assigned or priority based. The ability to allocate I/O channels at configuration or run time means that designers can decide how information is to be routed and which CEs should be employed after software development occurs. This takes some of the pressure off developers, who otherwise would have to write code simultaneously. In addition, there are other questions to be addressed: How many processors should the design start with? How should the CEs be connected? What are the priorities of the messages? And, how much memory is needed?



2. An array port on the crossbar can send and receive data to any of the five other ports. Each port on a crossbar is either a transaction initiator (master), recipient (slave), or intermediary.

Self-routing data packets can reduce latency, regardless of the application. The only overhead associated with self-routing traffic is the time required for control circuitry to read or write to address bits in a message header, typically in the 100-ns range as compared to the milliseconds needed for a typical bus data transfer. The reduced time interval results because the headers can be very short, typically less than 32 bits for a message that travels through up to four crossbars (the number typically required to connect any two CEs in a 256-processor multicomputer).

Transparent buffering of slave transfers to memory from external I/O applies to almost any scalable I/O system. The goal of this technique is to maximize the amount of bandwidth available for transfers between the processor and the memory in the CE by reducing the interference from traffic coming into the CE. That interference can be reduced by buffering in proportion to the speed difference between the CE's internal data

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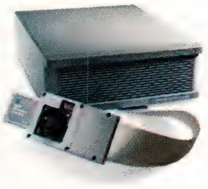

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COMPARISON OF BUS AND CROSSBAR TOPOLOGIES

Topology	Sustained rate (Mbytes/s)	Transfer time (ms)	Total corner-turn time (seconds)	Percentage of processing time
Bus	40	1.311	3.146	123
Bus	80	0.655	1.573	62
Bus	160	0.328	0.786	31
Bus	640	0.082	0.197	7.7
Bus	1280	0.041	0.098	3.8
Crossbar	150	0.350	0.189	7.4

path and the external traffic. The slower the external traffic, the longer the processor waits for the bus to clear. If this slow traffic can be buffered, it can be transmitted in bursts at the internal bus' speed. External I/O performance stays unchanged because the amount of data being sent in a given time interval is the same. For internal I/O, however, there's a performance improvement as external traffic spends less time on the bus.

Strategies like buffering external I/O and self-routing data make a strong case for the CE concept. The advantage to the CE technique is that although these features need only be designed in once, they can be leveraged repeatedly throughout the system, regardless of the application or scale. Other strategies, such as a broadcast capability, shared memory, and a mailbox interrupt system are more application-specific and designers may want to include them on a case-by-case basis.

Whether the broadcast function is of value depends on the proportion of messages that need to be received by a large number of CEs at the same time. If real-time data will be received by many CEs simultaneously, a broadcast capability is virtually mandatory. Broadcast also is recommended if there's lots of process synchronization and a resulting exchange of control flags. In a system with many processors, the alternative to broadcast is to update many CEs one at a time. Even if only one in a hundred transfers calls for broadcast, there can be a big win if that transfer can replace 100 individual transfers.

Shared memory makes sense in systems with a highly data-distributed I/O profile. Mandlebrat benchmarks offer a good measurement that scales well in systems with no shared memory, where a processor doesn't have to ask another processor for needed data. In those applications where CEs do have to share each other's data, however, the ability to directly access the remote CE's memory eliminates a software burden—negotiating with the remote processor. One way to implement shared memory is by employing a large flat address space and allocating portions to physically distributed memory locations. Another is to provide local address space that directly maps the remote memory space.

A mailbox interrupt subsystem offers greater configurability (and therefore scalability) in applications where many interrupts exist. Rather than use a shared-bus control line (which are limited), a mailbox subsystem signals interrupts using an array of dedicated memory locations. The receipt of a mailbox address tells the processor to stop what it's doing and execute the routine specified by the mailbox. The address on the mailbox points to an interrupt service routine located elsewhere in memory. There also may be content inside the mailbox itself that the processor uses to help execute the interrupt.

One advantage of mailboxes is that many boxes are available to handle the various interrupts. In addition, an interrupt can assign a specific task and processor. Therefore, only a small amount of overhead is associated with finding out where the interrupt is coming from and why it's being sent.

The slower the external traffic, the longer the processor waits for the bus to clear.

One architecture—the Raceway Interlink (developed by Mercury Computers)—employs these rules to implement a network of crossbars. Raceway is currently in the process of becoming an ANSI standard.

Crossbars and CEs can be incrementally added, subtracted, or reconfigured in response to growing, shrinking, or changing applications. Every transaction between CEs involves a port-to-port or crossbar-to-crossbar transaction. Each port on a crossbar is either a transaction initiator (master), recipient (slave), or intermediary. At any given time, a crossbar ASIC can receive simultaneous routing requests from 6 ports *(Fig. 2)*.

The ASIC contains arbitration logic that assigns a different priority to each of the different ports to avoid possible deadlocks. Each message has an associated programmable priority level that enters into the arbitration process. This allows requests from important transactions to be routed before those from less important transactions.

Data packets flow through the crossbar network based on routing data contained in the packet header. The header contains path information that lists a series of crossbar ports through which the header is to be routed. As the header transverses each crossbar, the crossbar logic shifts the route-path specification so as to expose the information to be used in navigating through the next crossbar. Once the route reaches the slave node, a circuit through the crossbar network is established. The master node can then read or write data through the established circuit.

The master can terminate the transaction when it's finished or when part of the path is needed by higher priority transactions. When the transaction is termi-

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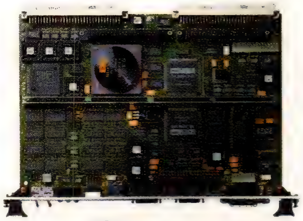

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nated, all the crossbar resources in the path are freed up for other transactions.

Routing information is contained in 32-bit words strobed onto a data bus on a crossbar port ahead of the address word and the data bits in the packet. The address word contains a lock bit, up to 31 address bits, and four width-alignment bits (address bits 3-27 are in the address word, bits 28-31 are in the route word). This lets the master access up to 16 Gbytes of slave address memory.

At each crossbar, a route word is shifted to the left to determine where the next packet goes. COntrol blocks within the routing specification include a broadcat-accept flag, a routing priority, and a broadcast-mode bit.

Driving the lock flag low creates a point-to-point connection between the master and slaves across the network, eliminating handshake latency. Other port requesters can't use any of the master's crossbar ports until it completes its block-transfer and releases its lock. The path-lock capability also is essential in certain multicomputer synchronization operations. Locked accesses are needed to support resource-sharing and processor-synchronization primitives, such as semaphores, and indivisible external-memory bus cycles, such as read-modify-write.

In addition to the 32-bit data bus, five other signal wires connect to each crossbar port. These provide port-to-port handshaking for functions that include ready-to-send address, ready-to-send data, ready-to-receive address, ready-to-receive data, and so on *(Fig. 3)*. Although all signals are synchronous (to a 40-MHz clock), transactions are asynchronous. Master and slave ports interact through request, grant, and ready signals that needn't follow a rigid time course.

A two-dimensional fast-Fourier-transform (FFT) application illustrates the benefits of I/O scalability. This useful signal-processing technique is used extensively in medical-imaging and pattern-recognition applications. The computational requirements are straightforward: a one-dimensional FFT operates on every row of an image, followed by an FFT on every column. Assuming that each processor in a multiprocessor configuration starts with rows, the 2D FFT interprocessor communication requirements become strenuous because a "corner turn" must occur—every processor exchanges data with every other processor.

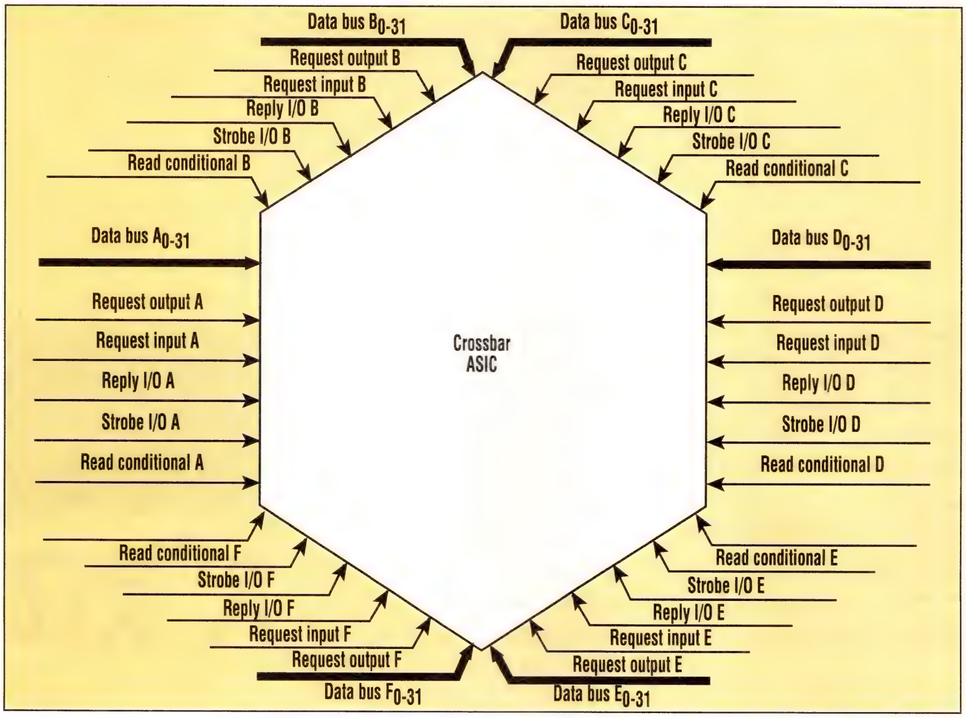
If there's a 4096 squared image, then the memory and processing requirements include: an image size of 16,777,216 complex pixels and 134,217,728 bytes; an image size/16 of 8,388,608 bytes (because it is split among 16 processors); an FFT time serially of 40.80 seconds; and an FFT time/16 of 2.55 seconds.

This configuration assumes a one-dimensional FFT time equal to 4.98 ms. If done on one processor, then 8192 FFTs would take 40.8 seconds. Hence, a problem of this size is more easily handled by multiprocessors. So, for this example, the processing is split among 16 processors. Ideal concurrency is assumed, with the best-case processing time of 2.55 seconds.

The corner turn on a bus can be calculated easily. Each of the 16 processors must do 15 transfers, for a total of 240 transfers. Because the topology is a bus, the transfers occur serially. Each transfer is 1/16 of each processor data set, or 512 kbytes. A time-transfer unit is the time required to transfer 512 kbytes, assuming different sustained rates *(see the table)*. For the calculation, assume a crossbar topology with a sustained transfer rate of 150 Mbytes/s and a time transfer of 3.5 ms. Because the maximum number of crossbars to transverse is three, the worst-case latency overhead is approximately 300 ns. That 300 ns is used in the calculations.

The same 240 transfers must take place, whether on a bus or a crossbar network. However, the crossbar allows parallel transfers. Because each terminal crossbar contains four processors (CEs), exchanging data among them requires 12 (4 × 3)

3. In addition to the 32-bit data bus, five other signal wires connect to each crossbar port to supply port-to-port handshaking for such functions as ready-to-send address, ready-to-send data, ready-to-receive address, and ready-to-receive data.



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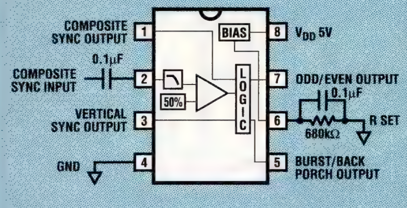
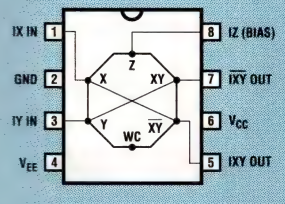


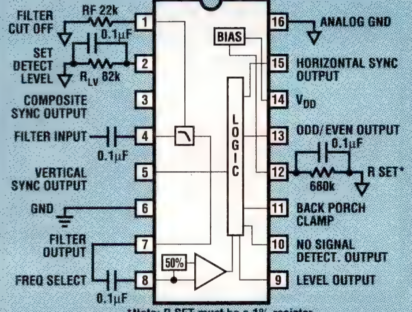
- Precision 50% Slicing
- Low Power CMOS (1.5 mA Max)
- $2.67 in 1,000's P-DIP

EL4083C
Current Mode 4-Quadrant Multiplier



- 200 MHz Bandwidth
- THD < 0.1% @ 10 MHz
- $6.90 in 1,000's P-DIP

EL4583C Video Sync Separator



*Note: R SET must be a 1% resistor

- Adjustable Filter & H-sync Output
- Precision 50% Slicing
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EL4441/EL4442
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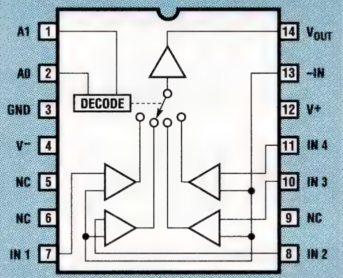

- 8 ns Switching Time
- 0.02%/0.02° Diff Gain/Phase
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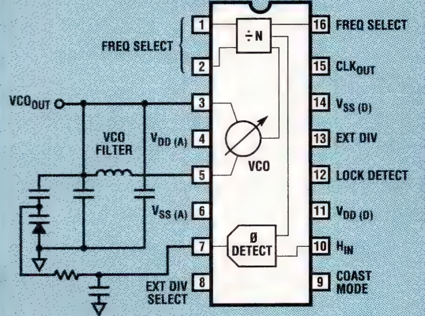
EL4584 Genlock



- Selectable 8-Preset Frequencies
- Precision Phase-Locked Loop
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EL4451C
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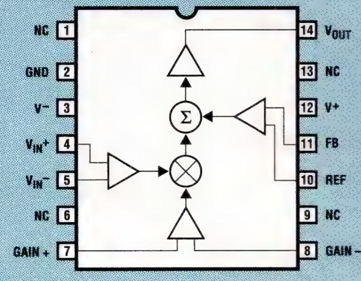

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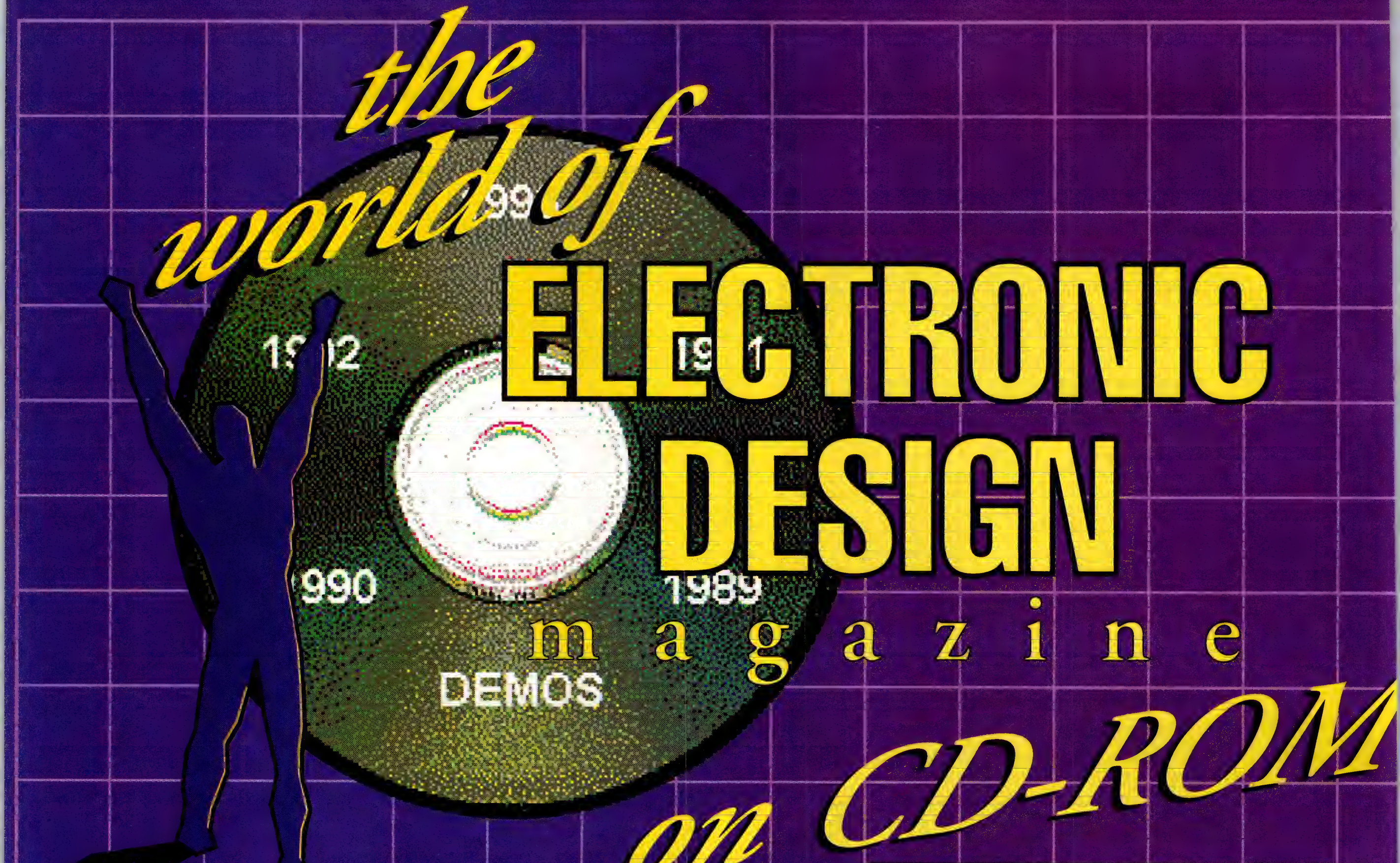

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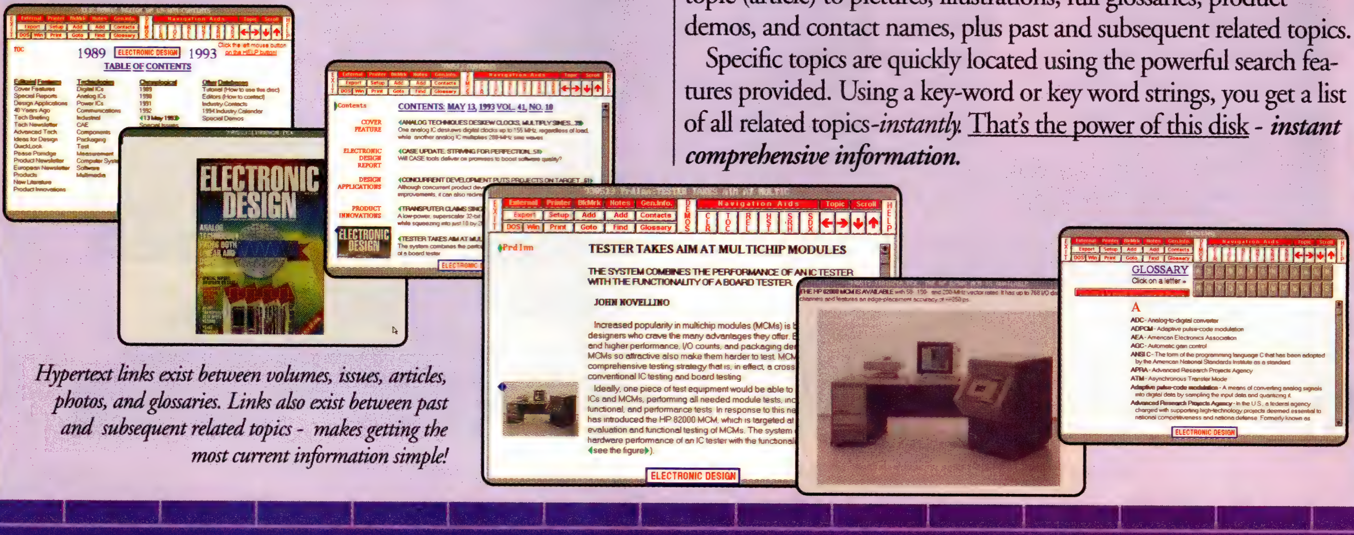

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1989 ELECTRONIC DESIGN 1993

Click the left mouse button on the HELP button!

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while squeezing into just 10 by 2

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The system combines the perfo
of a board tester

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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is b
designers who crave the many advantages they offer. E
and higher performance, I/O counts, and packaging de
MCMs so attractive also make them harder to test. MCM
comprehensive testing strategy that is, in effect, a cross
conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to
ICs and MCMs, performing all needed module tests, inc
functional, and performance tests. In response to this ne
has introduced the HP 82000 MCM, which is targeted at
evaluation and functional testing of MCMs. The system
hardware performance of an IC tester with the functional
see the figure).

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THE HP 82000 MCM IS AVAILABLE with 50-, 150-, and 200-MHz vector rates. It has up to 768 I/O d
channels and features an edge-placement accuracy of ±250 ps.

GLOSSARY
Click on a letter »

A

ADC - Analog-to-digital converter
ADPCM - Adaptive pulse-code modulation
AEA - American Electronics Association
AGC - Automatic gain control
ANSI C - The form of the programming language C that has been adopted by the American National Standards Institute as a standard.
APRA - Advanced Research Projects Agency
ATM - Asynchronous Transfer Mode
Adaptive pulse-code modulation - A means of converting analog signals into digital data by sampling the input data and quantizing it.
Advanced Research Projects Agency - In the U.S., a federal agency charged with supporting high-technology projects deemed essential to national competitiveness and national defense. Formerly known as

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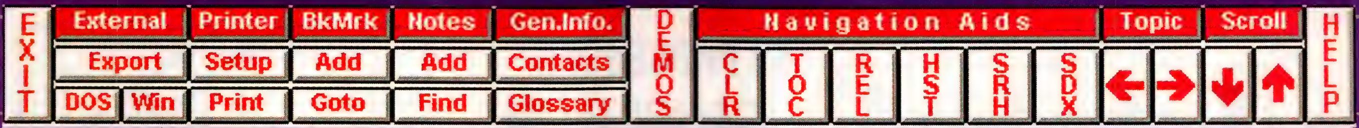
Hypertext links exist between volumes, issues, articles, photos, and glossaries. Links also exist between past and subsequent related topics - makes getting the most current information simple!



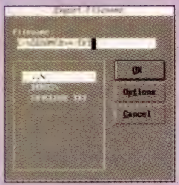
Learn the backbone of the Electronic Design Magazine CD-ROM interface - *the BUTTONBAR.*

Powerful, hypertext-based commands let you quickly and efficiently find, re-find, link, make notations, leave bookmarks, export, print, search, get product demos, and even return to your operating system!

EXIT - *Leaving so soon?*

The EXIT button quits the application, and takes you right on out into the cold, cruel, computer world. If you want to leave the Electronic Design Magazine, and still have easy access without re-launching, use the **DOS** and **Win** buttons. These are located under **External** *(see below).*

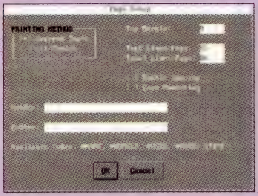
External - *Life beyond this disk*



The **Export** button will export any or all of an article based on your selection.

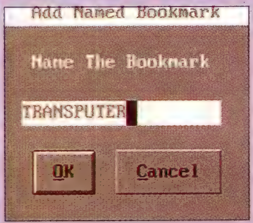
DOS & Win - **DOS** brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. Return to Electronic Design Magazine, where you left off, without re-launching.

Printer Commands



Setup & Print - Articles, editorials, glossaries, table of contents, illustrations, and photos (if your printer is capable).

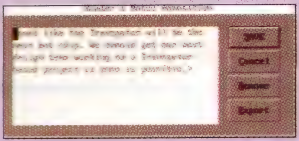
Bookmarks and Notes - *Leaving your mark*



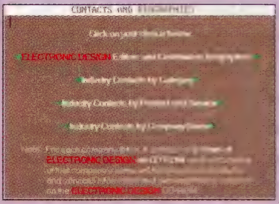
Name The Bookmark: TRANSPUTER

BkMrk - Bookmarks flag topics for future reference, just like using a bookmark in a real magazine. You mark a spot, and the bookmark is stored even if you quit. **GOTO** brings you back to your bookmarks. Deleting them is just as simple.

Notes - Add and find your own notations. Notes stay until you delete them, even after you quit.



Gen. Info - *Complete reference and more!*



Contacts are complete with company and contact names, phone numbers, and addresses. All of the information you'll need to follow up.

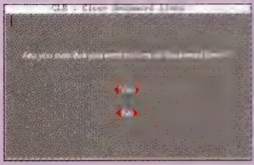
Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

DEMOS - *Instant products demos and information*

This button gives you pertinent product demos and information. Submitted by the manufacturer, demos often include live action footage, most in color.

Navigation Aids - *Magellan you're not, and you don't need to be*

All the aids you'll need to motor your way through this CD in no time flat.

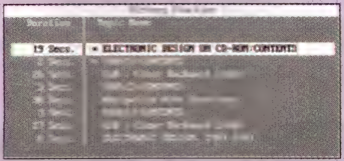


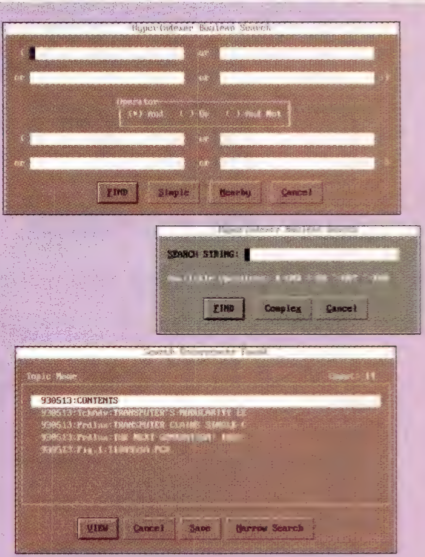
CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.

REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.





SRH - *Search* - Conduct simple, complex or proximity indexed searches.

SDX - *Subject Index* - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

Topic Keys - *Issue browsing*

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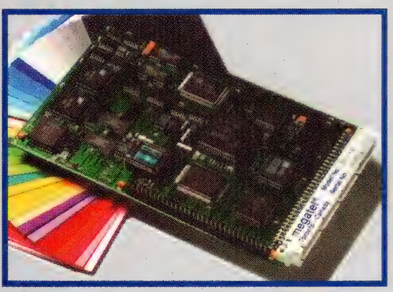

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transfers. However, two simultaneous transfers can take place on a terminal crossbar, so the 12 transfers occur in 6 time-transfer units.

There are four crossbars, each operating in parallel, and thus 48 transfers can occur in 6 time-transfer units. The remaining 192 transfers (240 – 48) are between CEs on different crossbars. Because each terminal crossbar can sustain two transfers, a total of four transfers can occur simultaneously between pairs. Collisions won't occur since the transfers can be routed whereby each of the four transfer paths use different crossbar ports on the intermediate crossbars at any one time. As a result, the remaining 192 transfers occur in 48 time-transfer units (192/4), providing a total of 54 (6 + 48) time-transfer units or 0.189 seconds.

Note the percentage of time—2.55 seconds—spent doing the corner turn over the parallel-processing time. Comparing performance, the crossbar topology is about equal to a 640-Mbyte/s bus. Again, the problem with such a bus is its inability to scale. Users wanting less than 16 processors must cover the same interconnect cost as a larger system. The crossbar topology can accommodate fewer processors simply by removing terminal crossbars. Scaling to 24 processors can also be done because the intermediate crossbars contain two available ports to connect to another two terminal crossbars.

Barry Isenstein, advanced product planning manager at Mercury Computer Systems, earned bachelor's and master's degrees in biomedical engineering at Case Western Reserve University, Cleveland, Ohio.

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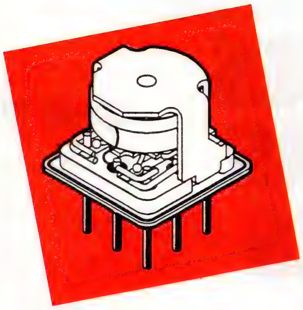

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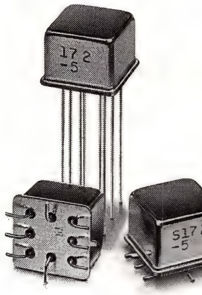

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READER SERVICE 130

SYSTEM DESIGN NEWS

Developers looking to convert their products to the Access.bus can take advantage of the Access.bus Peripheral Development Kit (PDK). The latest version of the kit, from Computer Access Technology Corp. (CATC), Santa Clara, CA, supports Revision 2.2 of the bus specification. Version 2.2 was recently released by the the Access.bus Industry Group, a consortium that maintains the standard. The kit, which runs on any standard PC, includes all the hardware and software needed to build an Access.bus peripheral that's compatible with Release 2.2. On a board that's got plenty of prototyping space is a programmable microcontroller, preprogrammed with Access.bus device-interface code. The kit also includes a PC-based add-on card that comes with system-level drivers and a monitoring program. The development kit sells for $1695. Included are device-driver and application-layer examples of implementing the generic Access.bus software protocol. CATC will also license the source code. Hence, developers can focus on specific project needs by having the device microcode. For more information, call CATC at (800) 909-CATC.

The VCOS real-time operating system, developed by AT&T Microelectronics, Allentown, Pa., provides full compatibility with the DSP extensions to the Microsoft Windows environment, enabling designers to create multitasking DSP subsystems. These subsystems will be compatible with any software written to Microsoft's DSP architecture interface, which was recently renamed the Resource Manager Interface (RMI), and includes I/O management and resource and concurrency management. Below the RMI are the hardware-specific functions, such as the board driver and DSP-chip-specific control functions. Thus, developers needing immediate multitasking for Windows 3.1 peripheral support applications can immediately adopt AT&T's VCOS. Moreover, once the enhanced version of SPOX, being prepared by Microsoft and Spectron Microsystems for the "Chicago" release of Windows (Windows 4.0), becomes available, they can develop additional applications or quickly port current ones thanks to the device-independent structure of the RMI. VCOS software also is compatible with the media-control interface, the Windows sound system, and standard communications drivers. Contact Lisa Brady at (610) 712-6496.

A family of PLL-based clock generators that deliver multiple clock outputs with skews under 500 ps at 100 MHz offer 16 programmable configurations and up to 18 outputs. One driver in particular, the 74FCT931 or FCT3931, is optimized for synchronous local-bus PC systems and comes in a 5-V or a "true" 3.3-V version, respectively. The circuits, designed by Integrated Device Technology, Santa Clara, Calif., are programmed via four select inputs to provide clock multiplication (2X, 3X), clock division (/2 or / 3), or clock inversion. A separate output-enable line allows all clock outputs to be disabled, reducing chip power drain when the clocks aren't needed. Both chip versions also have multiplexed reference inputs, which let the chips readily switch between different PLL clock sources. Also available are several 3.3-V clock drivers designed specifically to support the enhanced Intel 3.3-V Pentium, the IBM/Motorola PowerPC, and the latest MIPS-compatible CPUs. Based on a full 3.3-V-optimized process, the eight-output clock drivers can accept 5- or 3.3-V input signals, permitting the chips to serve as 5-V-to-3.3-V translators. The 74FCT388915 and FCT88915 drivers operate from 3.3 and 5 V, respectively, and deliver zero-delay clocks of up to 150 MHz with skews between outputs of less than 500 ps. A dual 1:5 fan-out clock driver (the 74FCT3805) with an output skew of 600 ps, and an ultra-low-skew 1:10 clock driver (the 74FCT3807) that provides an output skew of less than 350 ps, round out the family. Prices for the CMOS chips start at $7 each in 1000-unit lots for the 20-lead 74FCT3805 and at $10 each for the 56-pin SSOP-housed 74FCT931. Contact Kirby Kish at (408) 492-8319.

▼ VME ENGINE HOLDS FOUR SPARC CPUs

While maintaining 100% binary compatibility with the SparcStation 10 workstation family, the Sparc 10MP engine can support up to two TI SuperSparc or four Fujitsu hyperSparc processors on a 6U VMEbus card. The use of low-profile ECC memory-expansion modules lets system designers stack two modules, each ranging from 32 to 128 Mbytes. Other features include Ethernet, SCSI 2, and two serial ports, two SBus slots, and support for the Solaris 1.1 and 2.3 operating systems. Prices for the Sparc 10MP start at $12,995 with 32 Mbytes of DRAM.

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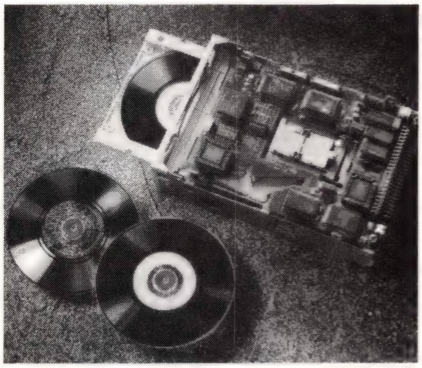
▼ MO DRIVE FEATURES 28-MS AVERAGE SEEK



The drawback to magneto-optical (MO) disk drives always has been their slow average seek times. That's now changing with the introduction of the LB3230, which boasts an average seek time of 28 ms. The faster seek is partly due to a 3600-rpm rate and a 256-kbyte buffer memory. Designed for both Apple and IBM-compatible platforms, the drive has an embedded SCSI interface that supports SCSI 2 commands and offers a 230-Mbyte capacity on a 3.5-in. cartridge. Reliability is improved by the drive's bundled self-test diagnostics and automatic calibration routines. Available now, the LB3230 MO drive sells for $800.

LaserByte Corp.
1330 Bordeaux Dr.
Sunnyvale, CA 94089
(408) 734-9200
▶CIRCLE 602

▼ SVGA MODULE HOLDS 68030/40 CPU

The GMS SVGA is an embedded super VGA single-board computer that can be customized for such real-time applications as process control and industrial automation. The board is configured with a Motorola 68030 or 68040 microprocessor. It can be built either with or without a VMEbus interface. A choice of single- or dual-access memory is available, in addition to simultaneous support of monochrome or color LCD panels and CRTs. A performance boost comes from the direct, non-arbitrated 32-bit data path between the VGA controller and the microprocessor. Up to 32 Mbytes of DRAM fit on the board. Software support is supplied for most popular real-time operating systems. Prices start at $1895.

General Micro Systems
8358 Maple Pl.
P.O. Box 3689
Rancho Cucamonga, CA 91730
(909) 980-4863
▶**CIRCLE 603**

▼ QIC DRIVE STORES 680 MBYTES, NATIVE

Like hard-disk drives, tape drives also are increasing in capacity and performance. The CTM 1360, which adheres to the QIC 3020 format, follows that trend. With a long-length tape, the drive can store up to 680 Mbytes of uncompressed data, 1360 Mbytes compressed. The transfer rate is 2 Mbits/s. The higher capacity comes from the use of thin-film magneto-resistive heads, which can handle the faster tape speeds. In addition, a higher-density tape is employed. The drive writes a series of servo information, called precision bursts, at the beginning and end of the tape to aid in the positioning of the head at high speeds. The drive maintains backward compatibility with earlier QIC-based drives.

Conner Peripherals Inc.
Tape Products Group
1650 Sunflower Ave.
Costa Mesa, CA 92626
(714) 966-5580
▶**CIRCLE 604**

▼ RECONFIGURABLE BOARD AIDS CUSTOM DESIGNS

Designed for custom computing applications and logic prototyping, the X12-3000 reconfigurable hardware system features support for 12 Xilinx 3000 series FPGAs. Each of those modules can be individually programmed to operate independently from the others in the system. In addition to the local SRAM that's attached to each FPGA, the board contains two sets of global memory. The first block is high-speed SRAM that stores local state information from the system controller or interfaces with the PC or individual FPGAs. The second block, which holds up to 16 Mbytes of DRAM, is a SIMM. Bundled software contains command-line routines to configure the FPGA array and manage data transfers to and from the board.

National Technology Inc.
9500 South 500 West
Sandy, UT 84070
(801) 561-0114
▶**CIRCLE 605**

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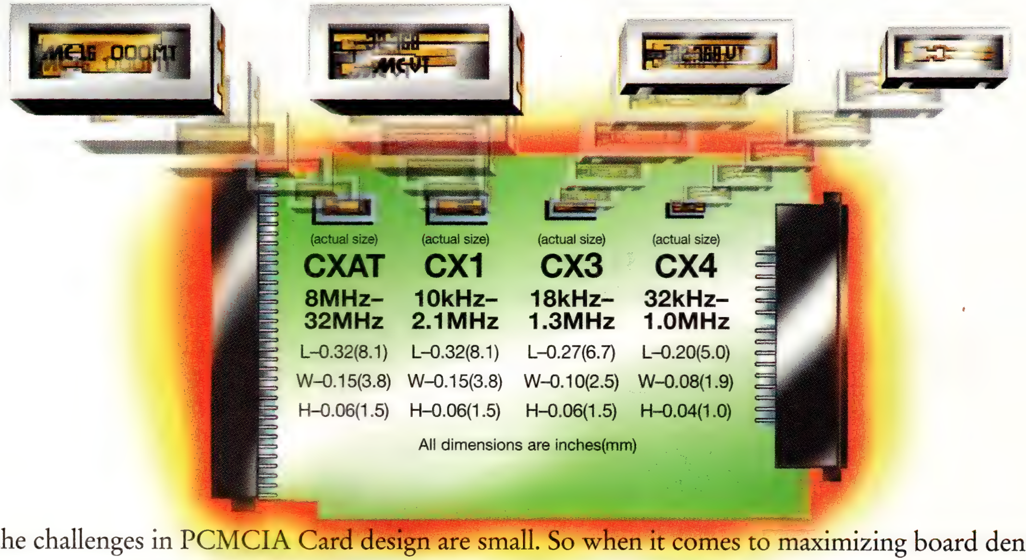

(actual size)	(actual size)	(actual size)	(actual size)
CXAT	CX1	CX3	CX4
8MHz–32MHz	10kHz–2.1MHz	18kHz–1.3MHz	32kHz–1.0MHz
L–0.32(8.1)	L–0.32(8.1)	L–0.27(6.7)	L–0.20(5.0)
W–0.15(3.8)	W–0.15(3.8)	W–0.10(2.5)	W–0.08(1.9)
H–0.06(1.5)	H–0.06(1.5)	H–0.06(1.5)	H–0.04(1.0)

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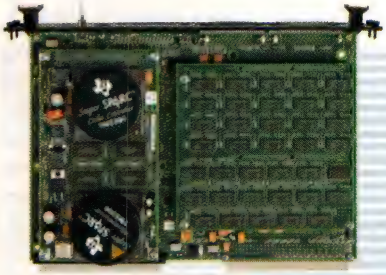

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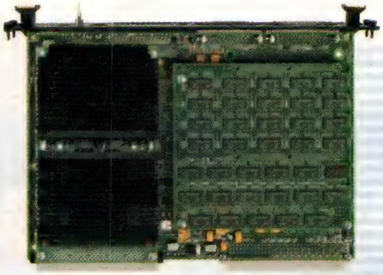

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- **2817-3414 SPECrate_int 92**
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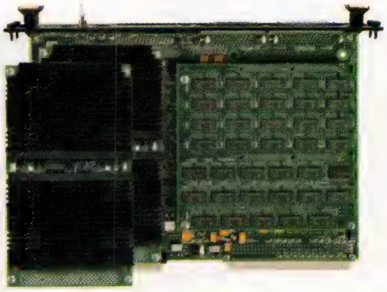

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▼ PC MOTHERBOARD HOLDS ALPHA CPU

PC designers can get higher performance using the AXPpci33, a motherboard that's based on the 64-bit Alpha AXP RISC family of microprocessors. Six different configurations are available. The 21068 CPU runs at 66 MHz and the 21066 runs at 166 MHz. Each processor can sit on a board with no cache memory, or 256 kbytes or 1 Mbyte of cache memory. The board also is based on the PCI local bus. Seven additional expansion slots allow for system customization. Performance ranges from 31 to 70 integer SPECmarks. In addition, the board conforms to most standards and operating systems, including Microsoft Windows NT and Unix. Volume shipments will start this summer. Large quantity prices for the AXPpci33 fall under $500.

Digital Equipment Corp.
2 Results Way
Marlboro, MA 01752
(800) DIGITAL.
▶ CIRCLE 606

▼ AT MOTHERBOARD FITS ON TINY MODULE

Designers of handheld computers and other portable equipment can take advantage of the CARDIO-X86, a credit-card-sized motherboard that ranges in speed from 8 to 14 MHz. The card contains the CPU, I/O controllers, CGA graphics, flash ROM for BIOS, and DRAM. It measures 85.6 by 54 mm and contains direct support for an LCD display, hard and floppy disk drives, and a keyboard. The CARDIO-X86 connects to outside devices through a 236-pin connector. It also incorporates an XT-bus and a proprietary interface, Epson's All-In-One System Interface (EASI), to simplify system upgrades. In large quantities, the card costs under $300. The base configuration consists of the CPU, 1 Mbyte of DRAM, and 256 kbytes of ROM.

Epson America Inc.
20770 Madrona Ave.
Torrance, CA 90509
(310) 782-5184
▶ CIRCLE 607

▼ 64-BIT GRAPHICS BOARD RIDES PCI BUS

As 32-bit graphics accelerator cards that fit into the PCI bus become mainstream, the recently developed Nitro PCI goes to the next plateau. Simply put, it can handle 64 bits. Based on the CL-GD5434 video controller-accelerator from Cirrus Logic, the board keeps pace with VRAM-based solutions while maintaining the cost level of a DRAM-based board. The accelerator chip integrates a 64-bit GUI engine, 64-bit internal data paths, and a 64-bit framebuffer interface, resulting in a performance level greater than 13.5 million pixels/s. The board comes in 1- and 2-Mbyte configurations to handle up to 65,536 colors with 1024 by 768 pixels noninterlaced. The 1- and 2-Mbyte Nitro PCI boards sell for $179 and $249, respectively.

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Richardson, TX 75081
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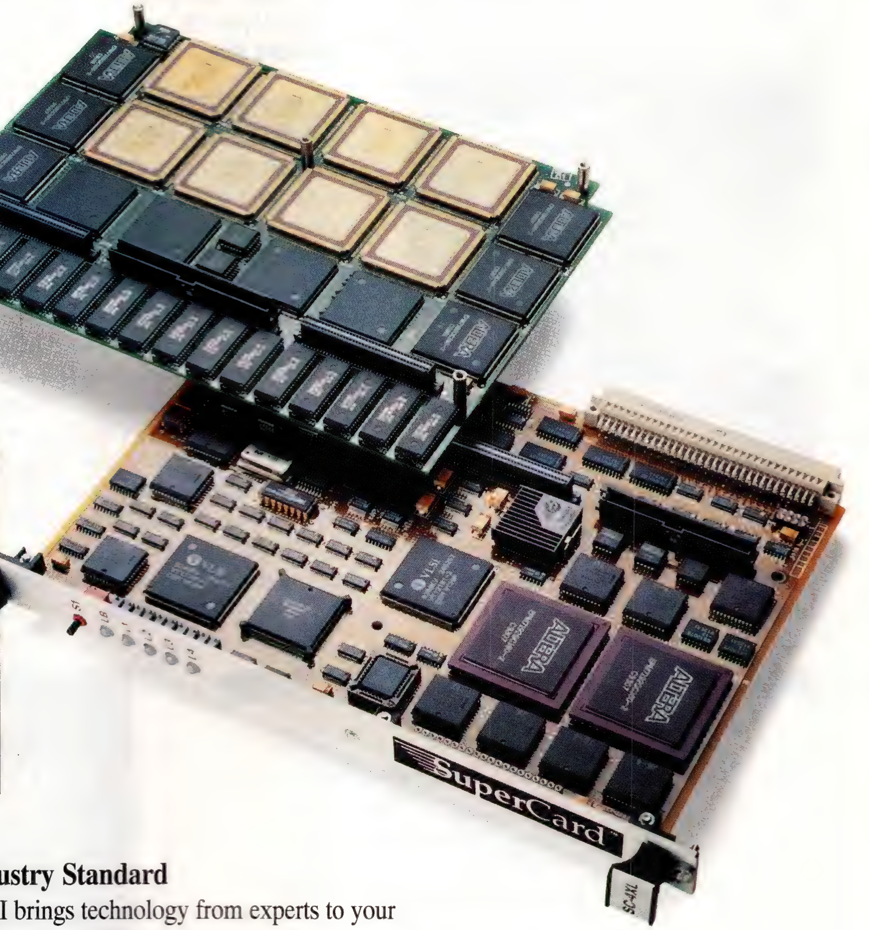
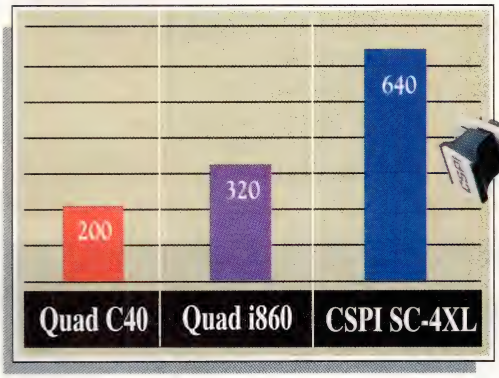
The Logical Choice for Multiprocessor Power – SuperCard-4XL Architecture



Million floating point operations per second on 6U VME board



Fastest Hardware

The need for processing power is insatiable for real-time multiprocessing solutions in defense, industrial, and medical applications. Greater resolution, faster I/O, larger data sets, and higher throughput all require signal and image processing technology pushed to the limit.

The SuperCard-4XL fulfills these needs – it's fast, compact, and very reliable! In fact, CSPI is the only vendor today offering up to 640 MFLOPS in a single 6U VME slot.

Our method is simple – group eight processors in pairs to create four processing elements on board. Hand coded library functions offer transparent access to this pipelined parallelism.

Best Value

With a list price of $47/MFLOP, we make no compromises to provide the maximum density of floating point power at the lowest price. And, with over 3,000 SuperCards operating in the field, reliability is assured.

Industry Standard

CSPI brings technology from experts to your program team. Our partners range from industry recognized leaders to distinguished younger companies. Select CSPI's open software solutions for real time multitasking/multiprocessing C and Ada development, plus graphical programming capabilities and a new parallelizing interface.

CSPI's commitment to hardware standards is designed into the SuperCard Family.

- VSB connectivity is maintained on board for compatibility with third party products
- VME64 is included for maximum bandwidth on the system bus
- National Semiconductor's QuickRing technology is selected for scalable high-speed board-to-board interconnect

MIL-spec

Our MIL-spec partner, Hughes Aircraft Company has developed a SuperCard XL model for MIL-spec environments.

Capture the Power

Call Susan Snell Solomon at **1-800-325-3110** and we'll demonstrate how SuperCard power can be harnessed by your application. A copy of our white paper *Scalable Interboard I/O for Multiprocessing DSP Applications* is yours for the asking.

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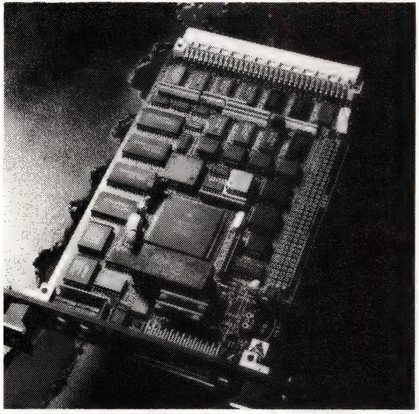
▼ CPU BOARD FITS IN TIGHT SPACES

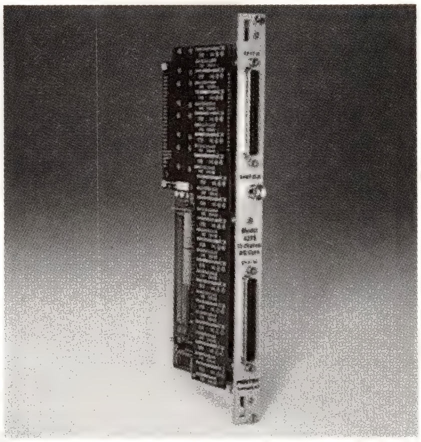
Designed for space-sensitive industrial applications, the SAC 340 is a single-size Euro CPU card. Based on an MC68340 microcontroller, the board can regulate the CPU's frequency to reduce power consumption. It comes with 2 Mbytes of battery-backed SRAM and 1 Mbyte of flash EPROM. Other features include two bidirectional 8-bit parallel ports and two serial channels. An extension sits on the card for customization through a 96-pin connector. A wire-wrap board is available to simplify the design.



American Eltec Inc.
4340 Stevens Creek Blvd.
Suite 204
San Jose, CA 95129
(408) 244-4700
▶ CIRCLE 609

▼ CONVERTER BOARDS HANDLE 32 INPUTS

Designed for embedded DSP applications, the 4275 and 4375 digital-to-analog converters feature 32 individual delta-sigma converters with 16-bit resolution, sampling rates up to 100 kHz, and built-in conditioning. The difference between the two cards, which are based on the AD776 chip from Analog Devices, is that the 4275 is built for the VMEbus, while the 4375 connects to the Multibus. They're suited for such real-time applications as medical instrumentation, imaging systems, radar and sonar, speech processing, communications, data compression, and embedded control. Each of the 32 inputs is buffered by an amplifier stage that supplies a ±5-V full-scale input voltage range. Front-panel multi-pin connectors offer a convenient method of attaching signal inputs through a flat-panel ribbon connector or discrete wiring harness.



Pentek Inc.
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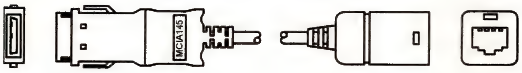

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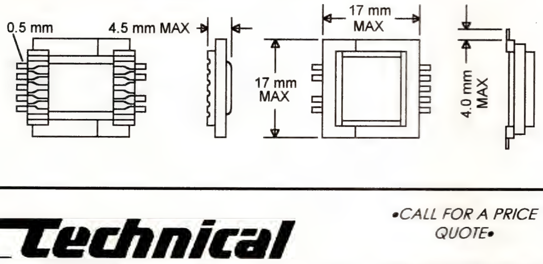

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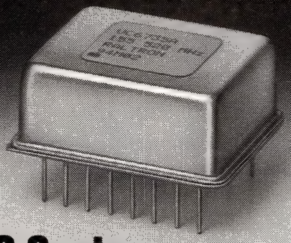

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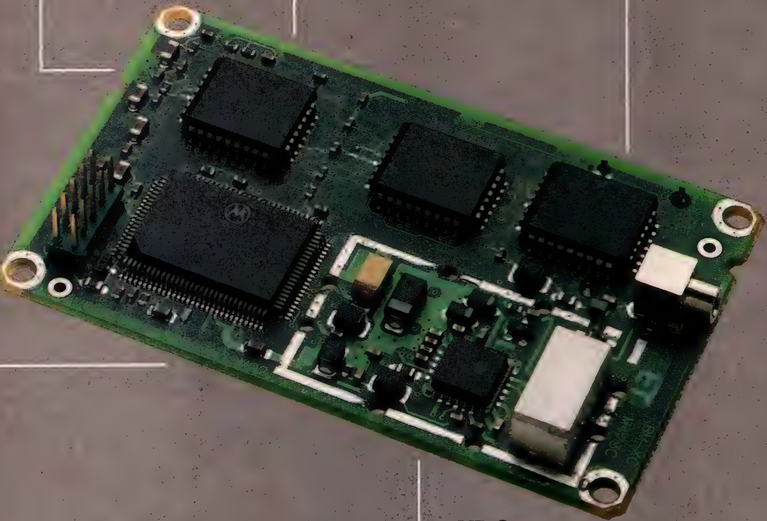

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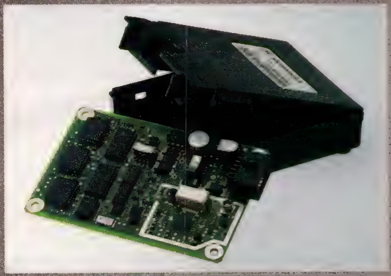

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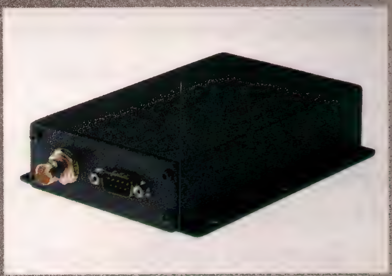

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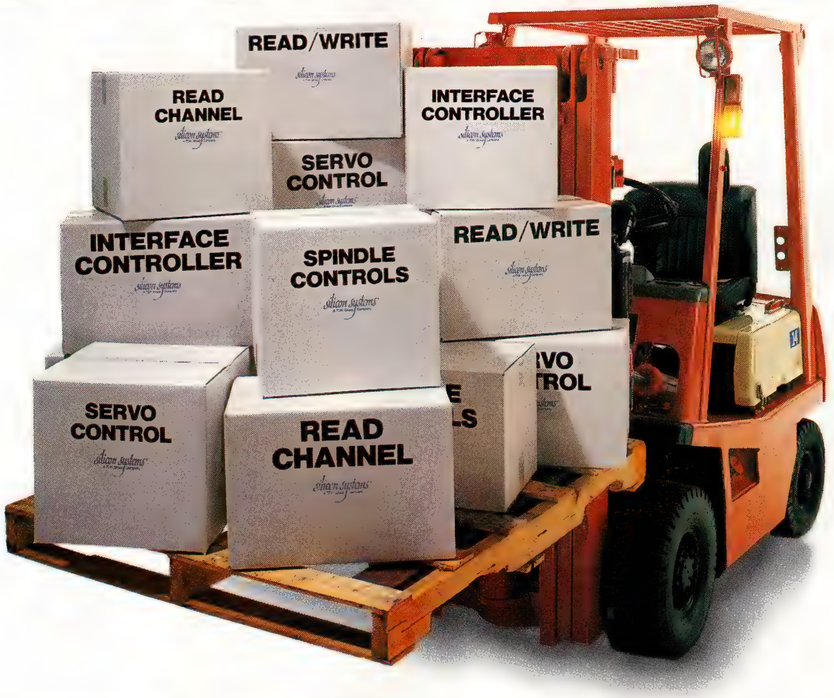

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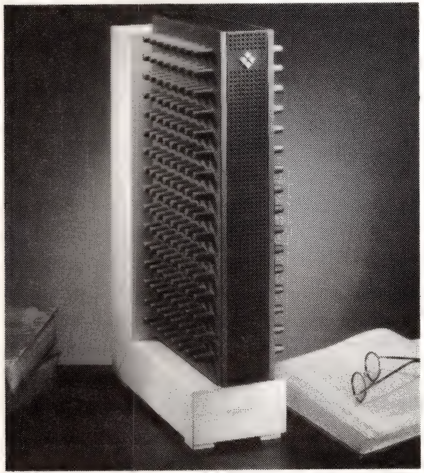
▼ PARALLEL SYSTEM TAKES ON POWERPC

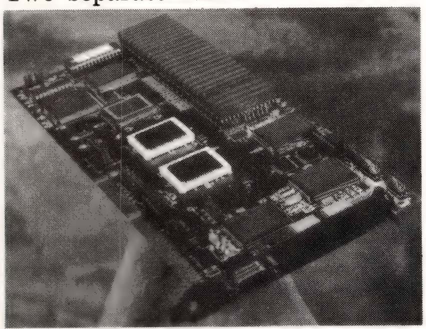
The PowerPC microprocessor is becoming the CPU of choice for many applications. The PowerXplorer employs the chip in conjunction with a Transputer in a parallel-processing application. With 4 to 64 nodes, the board delivers up to 10 GFLOPS. Each node holds an 80-MHz PowerPC 601 processor and 8 or 32 Mbytes of memory. The transputer adds 30 MIPS and 8.8 Mbytes/s of intelligent communication bandwidth per node. The system is bundled with compilers, utilities, and PARIX, a Unix derivative that's customized for massively parallel systems. The PowerXplorer is currently shipping, with prices starting at under $40,000.



Parsytec Inc.
245 W. Roosevelt Rd.
Bldg. 9 Unit 60/61
West Chicago, IL 60185
(708) 293-9500
▶ CIRCLE 611

▼ MUTLIMEDIA BOARD RUNS REAL-TIME VIDEO

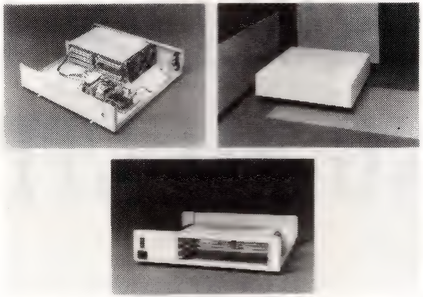
Two separate full-motion video inputs, one live and one compressed, can be sent to a PC to display four simultaneous moving images using the MegaMotion video card. The board supplies full image-capture capability with real-time 30-frame/s video capture at a resolution of 320 by 240 pixels. JPEG video compression is used to improve disk utilization for image storage. Compression ratios can be altered to meet the user's image-quality and storage requirements. Designed for professional-quality industrial video presentations, business multimedia, communications, and home-video applications, the board can show up to 16 customizable frames by displaying combinations of live video and freeze-frame images in real time. A complete array of professional editing special effects are included. Available now, the MegaMotion multimedia board sells for $1295.



Alpha Systems Labs Inc.
2361 McGaw Ave.
Irvive, CA 92714
(714) 252-0117
▶ CIRCLE 612

▼ LOW-COST ENCLOSURES ADD FLEXIBILITY

The Series L enclosures gives designers added flexibility when configuring their VMEbus systems. The family holds from one to five boards, a 110- or 200-W power supply, a card cage, dual fans, and an eight-layer backplane that incorporates active automatic daisy chaining. To supply easy access to internal components, the enclosures are designed so that all controls, including those on the VME boards, are readily available at the rear of the enclosure. By removing two screws, the whole top and sides slide off. The smallest of the family, with just one slot, measures 1.9 in. high by 16 in. wide by 16.06 in. deep. Prices for the Series L enclosures start at under $1000.



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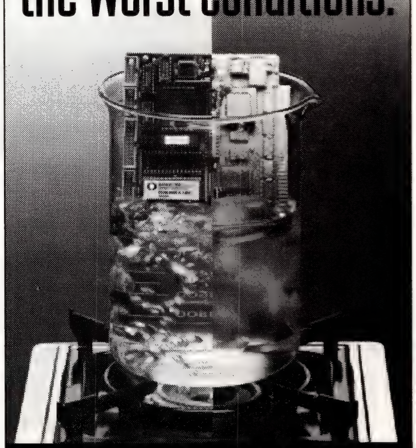

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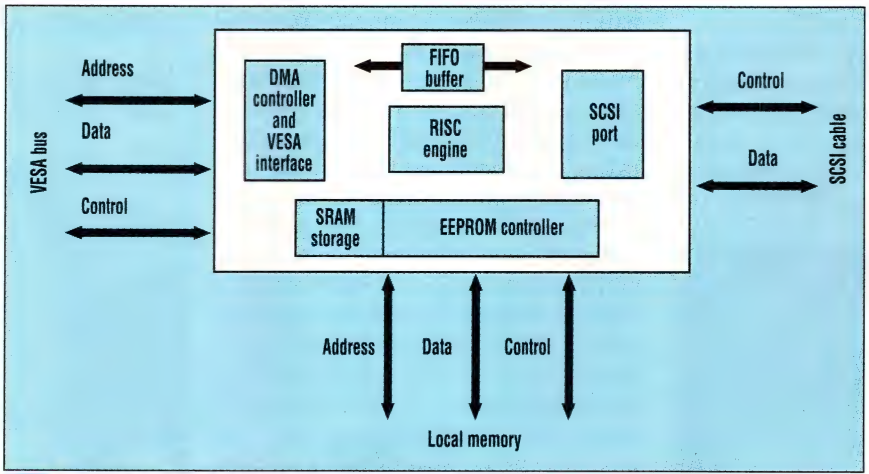


1. SIX MAJOR BLOCKS hold the main functions on the ASC1000/1200 multithreading SCSI controller designed by AdvanSys. The optimized RISC processor, the controller's heart, is surrounded by the SCSI port interface, on-chip RAM (ASC1200 only), EEPROM control logic, a DMA controller and VESA bus interface (ASC1000), and a FIFO buffer. Off-chip EEPROM can be used to retain the control programs for the RISC engine. Upon boot-up, the EEPROM contents are loaded into the ASC1000/1200's local RAM.

MULTITHREADING DEVICE COMBINES A DEDICATED AND OPTIMIZED RISC CPU WITH A BYTE-WIDE INTERFACE.

SCSI CONTROLLER EXCELS IN HANDLING MULTITASKING

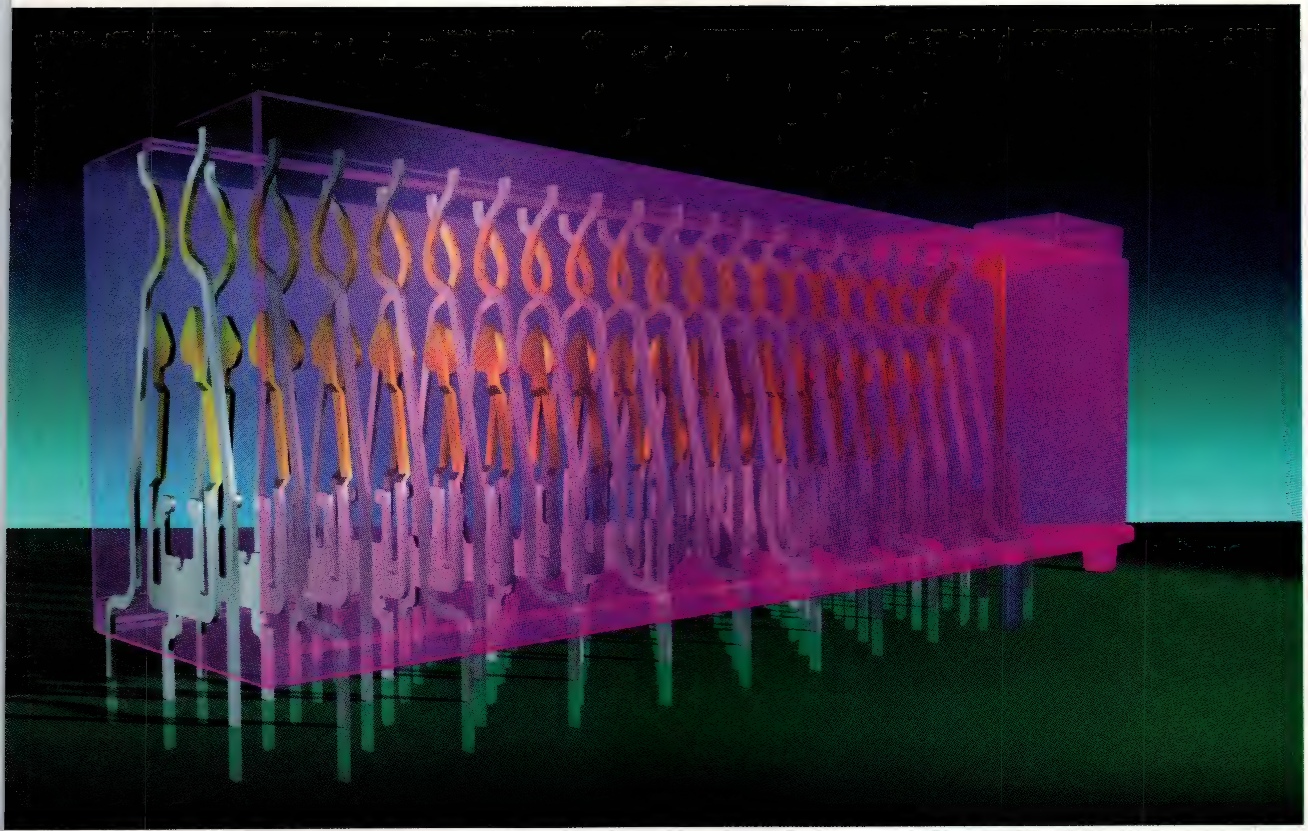
DAVE BURSKY

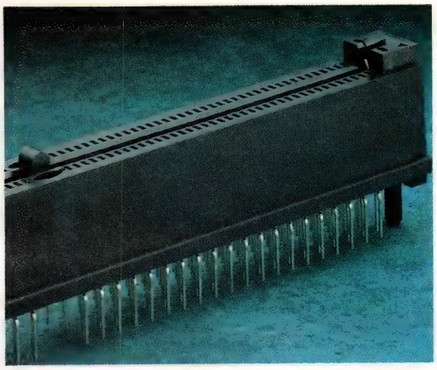
The small-computer system interface (SCSI) provides a simple, high-performance interface in single-tasking applications. Standard SCSI controllers, however, deliver less than optimal performance as more demanding applications start to run concurrently and as storage subsystems are forced to deal with multitasking. This prompted designers at AdvanSys to craft a new controller that's designed from the ground up. The device efficiently handles multitasking applications, combining the processing horsepower of a dedicated and optimized RISC CPU with a high-performance byte-wide SCSI-2 controller interface.

The ASC1000/1200 controller forms the heart of a family of SCSI host adapters. It packs about 18,000 gates, 2000 of which form the RISC engine. The first version, the ASC1000, a 160-lead, plastic QFP, ties directly into the Video Electronic Standard Association (VESA) local bus (VL bus), or can be used on a host's motherboard. A second version, the ASC1200, interfaces directly to the peripheral-component-interconnect (PCI) bus.

Besides the RISC engine that coordinates all chip activities, the ASC1000/1200 have a DMA

How to hit 500ps rise times with card edge economy.





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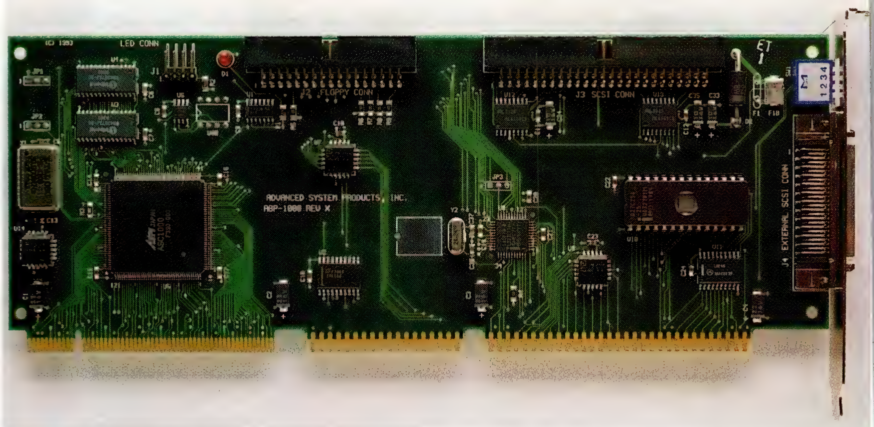
READER SERVICE 195

interface for high-speed data, and support multithreaded program needs *(Fig. 1)*. The RISC engine handles the rapid handshakes with the various SCSI peripherals, while the DMA bus-master transfers data between the SCSI device and main system memory, bypassing the internal buses of the SCSI controller. That allows transfers to occur at host-bus speeds, minimizing data-transfer delays.



2. LITTLE SUPPORT **beyond a crystal oscillator, off-chip nonvolatile memory (EEPROM, EPROM, etc.), and a few simple logic chips is needed by VLbus boards based on the ASC1000 multithreading SCSI controller. That's because the VESA-bus host-system interface is built into the ASC1000.**

Both chips have three I/O ports: one to the host interface, one for the local memory, and one for the SCSI interface. Each transfers synchronous data at 10 Mbytes/s over the SCSI bus. Bus arbitration, Message ID, Tag Message, and Command Transfer operations all can be completed in 12 µs. Furthermore, a new SCSI request can start within 10 µs once the current SCSI operation is finished. In addition, the host processor is able to start a SCSI request in just 5 µs thanks to the host-accessible local memory's shared-memory communication.

Multithreading permits the chip to process up to 255 simultaneous requests, reducing SCSI-bus idle time. Most other SCSI controllers are limited to handling about 16 simultaneous active threads. For SCSI-1 devices, there can be only one outstanding request on each device; for SCSI-2 devices, multiple outstanding requests (so-called queuing of multiple commands) are permitted on each device. As a result, both ICs can send more simultaneous requests to SCSI-2 devices on the SCSI bus, at several times the throughput of most previous-generation SCSI controllers.

Both chips also can process 255 simultaneous requests without intervention from the host, storing all requests in its local RAM (off-chip for the VL version, on-chip for the PCI version). The RISC engine scans the RAM to find available requests and then sends requests to SCSI devices, performing SCSI handshakes without host intervention. The processor, which executes a program stored in the local RAM, needn't access the external system bus to execute its operations. The same RAM also holds all requests from the system software.

That RAM is typically loaded during system initialization from either an off-chip EEPROM or from the host memory. The software initializes all internal variables and sets up the proper device drivers to control the specific I/O devices attached to the SCSI bus. Although the device drivers support DOS, Windows, Novell Netware, OS/2, and Unix, the on-chip RAM allows users to tailor their own driver and upload it into the RAM.

The built-in DMA controller provides a 27-bit address as the bus master. It includes a 27-bit transfer counter and a 128-byte FIFO buffer. Data is transferred on the SCSI port over an 8-bit, 10-Mbyte/s single-ended SCSI channel. Six bus clocks are needed for every 16 bytes of main-system-memory read (burst mode)_ equivalent to 33 Mbytes/s at a 50-MHz clock.

The flexible SCSI control provides a 15-byte synchronous transfer offset, and automatic Request-Sense command execution. Typical SCSI operations require no host intervention. On the other hand, concurrent SCSI commands cause less than one host interruption per SCSI command. And for diagnostics, internal registers can be accessed and read or written to by the host. The RISC engine can be single-stepped through its instruction-execution sequence, easing software or hardware debugging. A watchdog timer prevents extended system hangups due to malfunctioning I/O devices.

The first VL-bus boards with the ASC1000 will be offered by AdvanSys itself *(Fig. 2)*. The cards support the VL-bus burst mode, transferring data at up to 120 Mbytes/s. Transfers occur on SCSI at 10 Mbytes/s in the synchronous burst mode (Fast SCSI), at 5 Mbytes/s on the standard SCSI mode, and at 3 Mbytes/s in the asynchronous mode. Moreover, the controller can handle over 1700 scatter-gather segments without burdening the host CPU's system bus.The card is compatible with the SCSI-2 version of the SCSI standard and supports up to seven SCSI devices.

The card is available in two "kit" bundles, one aimed at multimedia systems and the other targeted at network nodes. Multimedia kits include the Corel SCSI version 2 as well as utilities for Photo CD, Audio CD, CD-ROM writers, scanners, and backup devices. The network version includes Corel's complete network-manager software, which lets the host implement fault-tolerant RAID level 4 and 5, a CD-ROM server with caches, advanced jukebox support, and support for optical devices on a server. ☐

PRICE AND AVAILABILITY

In lots of 1000, the ASC1000 or 1200 RISC-based SCSI controller chips sell for $21.95 each, while the single-unit prices for the board "kits" will be set at $379 for the multimedia version and $599 for the network version. Samples of both the chips and boards are available from stock.

AdvanSys Inc., 1150 Ringwood Ct., San Jose, CA 95131; Lou Williams, (408) 383-9400. **CIRCLE 511**

HOW VALUABLE?	**CIRCLE**
HIGHLY	527
MODERATELY	528
SLIGHTLY	529

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READER SERVICE 190

PCI BUS LINKS DIRECTLY TO PROCESSOR BUS

HIGH-PERFORMANCE PCI CONTROLLER OPERATES IN BUS-MASTER OR SLAVE MODE.

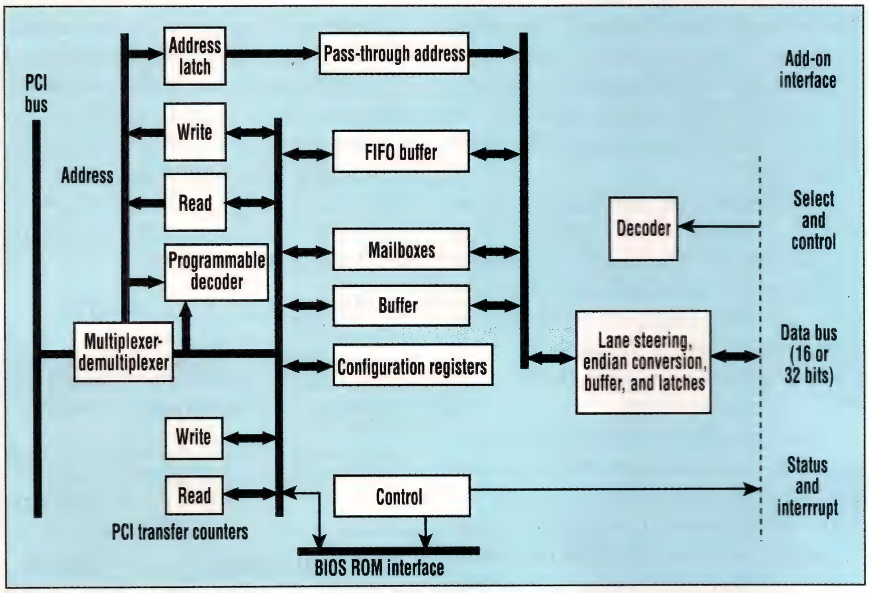
RICHARD NASS

The PCI local bus offers attractive features to PC users. Its 120-Mbyte/s bandwidth (132 Mbytes/s peak), for example, is significantly higher than that of the standard ISA bus. In addition, a local bus moves peripherals off the I/O bus and sets them closer to the system's processor bus for increased data-transfer rates. Moreover, when all of the pieces are finally put in place, the PCI bus will give end users something that's been discussed for some time—plug-and-play capability.

Systems have been designed with the PCI bus in volume quantities for about six months. But most are built with ASICs and lots of glue logic that ties the local bus into the rest of the system. The S5930-33 master/slave controller interface developed by Applied Micro Circuits Corp. (AMCC), San Diego, Calif., however, offers designers a standard part that simplifies the overall design while reducing the system's time-to-market.

The single-chip solution supplies a high-performance interface between the PCI bus and custom add-in cards. It supports several layers of interface sophistication, and at the lowest level can operate as a PCI bus target. For high-performance applications, the device can become the bus master. Address decoding and sourcing, burst transfers, and all of the logic needed to perform efficient data transfers are integrated into the device.

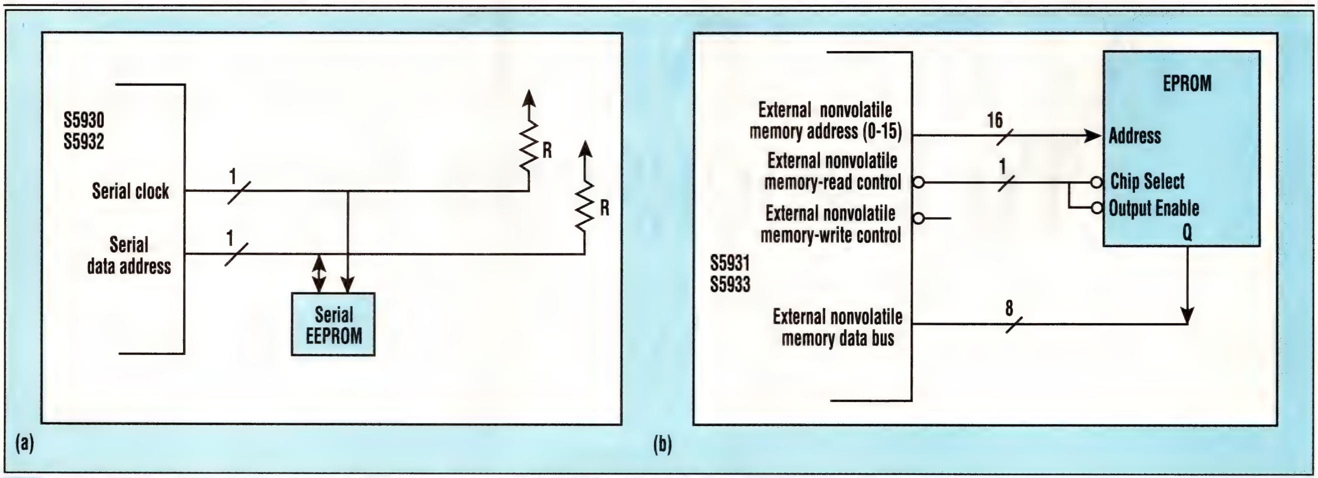
Included on the chip is a bidirectional 32-bit-wide FIFO buffer that facilitates the system-to-system synchronization and data transfers between the local bus and the peripheral board. A custom BIOS EPROM is able to perform any pre-boot initialization that the peripheral requires. The external memory (ROM, EPROM, or nonvolatile RAM) can be in either "by-eight" or serial form.



1. DATA MOVEMENT ON the S5930-33 PCI controller can occur between the PCI and add-on buses through the FIFO buffers or mailbox registers. FIFO transfers are handled through software control or hardware, using the controller as a bus master.

DIRECT CONNECTION

The part permits direct connection between the local bus and various general-purpose microprocessor-style buses. Bus-master transfers can be performed on the local bus while accesses occur simultaneously on the peripheral board's processor bus. Transfer parameters, such as the PCI address, transfer counts, mailbox registers, and status, are supplied in the interface controller as I/O-


S5930
S5932
Serial clock
1
Serial data address
1
R
R
Serial EEPROM
(a)
External nonvolatile memory address (0-15)
16
EPROM
Address
External nonvolatile memory-read control
1
Chip Select
Output Enable
Q
External nonvolatile memory-write control
S5931
S5933
External nonvolatile memory data bus
8
(b)

2. ONE DIFFERENCE AMONG THE FAMILY MEMBERS involves the type of nonvolatile memory that's employed. The S5930 and S5932 can handle a serial device (a), while a byte-wide device operates with the S5931 and S5933 (b).

mapped locations on the PCI bus.

The S5930-33 consists of three physical bus interfaces: the PCI bus, the add-on bus, and an optional external nonvolatile memory *(Fig. 1)*. Data movement can occur between the PCI and add-on buses or the PCI bus and the nonvolatile memory. Transfers between the two buses can pass through the FIFO buffers or mailbox registers, or the transfers can utilize a pass-through data path. FIFO transfers on the PCI bus interface can be done either through software control or hardware, using the S5930-33 as a bus master.

The controller's mailbox registers offer a bidirectional data path that can send data or software-control information between the host and the PCI peripheral. The mailboxes serve as customizable command, status, and parametric data registers. However, the application software defines the actual implementation of the mailboxes. They often can initiate larger data transfers over either the FIFO or pass-through data paths. Interrupts can be configured to occur on the PCI and add-on buses based on specific mailbox events.

The chip holds two separate FIFO data paths. One handles data movement from the PCI bus to the add-on bus, while the other handles movement in the opposite direction. Both FIFOs support bus mastering and each has an address pointer and transfer-count register associated with every PCI-bus transaction. Various endian translations can be performed when data is moved through the FIFO. As a result, each add-on board can maintain a fixed endian structure, while the system operates in its own native endian format.

JUST PASSING THROUGH

With the add-on interface, the pass-through feature allows actual PCI-bus transactions to be executed in real time. The feature also helps achieve high-performance burst transfers between the PCI bus and add-on-bus external peripherals or memory devices. In the pass-through mode, the controller offers the benefits of the configuration registers and full PCI compliance, while permitting customization and flexibility when implementing add-on boards.

The pass-through logic consists of one address register and two data registers (one for each direction). Control information needed to define the current PCI-bus transaction is given to the add-on interface on dedicated pins.

The S5930-33 serves as an endpoint within a given PCI system. This means that it's the beginning and/or final point in a data transfer. As a bus agent, the chip must support the configuration registers to supply a standardized method for software to integrate add-on functions.

The controller's 32-bit add-on-bus interface completes transfers to and from its internal registers through a chip-select decode in conjunction with a read or write signal. The chip supplies dedicated pins that let its FIFO buffers operate with custom DMA ports or additional external FIFOs.

The output pins on the add-on interface include an interrupt source, a buffered clock, and a software-controllable reset. The interrupt output pin signals when a selected mailbox or self-test event is sent from the PCI interface. The buffered clock output synchronizes the pass-through data transfers, while the software-controllable reset provides a means for add-on hardware to handle a system reset.

The nonvolatile interface makes it possible to customize the chip. It also offers access to an optional BIOS ROM on the PCI bus. The nonvolatile memory can take the form of either a serial or byte-wide device. Serial devices can range from 128 to 2048 bytes, while the byte-wide type can vary from 128 bytes to 64 kbytes.

There are four parts in the family. The S5930 and S5931 are built with a 16-bit bus, while the S5932 and S5933 employ a 32-bit bus. In addition, the parts are further differentiated by the nonvolatile interface. The S5930 and S5932 can handle a serial device, while a byte-wide device operates with the S5931 and S5933 *(Fig. 2)*.☐

PRICE AND AVAILABILITY

The S5930-33 master/slave controller is priced at $39.95 each in lots of 1000. Sample quantities will be available in July, with production quantities scheduled for the fourth quarter.

Applied Micro Circuits Corp., 6195 Lusk Blvd., San Diego, CA 92121; (619) 450-9333.

CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	530
MODERATELY	531
SLIGHTLY	532

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READER SERVICE 98

IC BRINGS WORKSTATION 3D GRAPHICS TO PCs

THE LOW-COST SINGLE CHIP WILL PROVIDE UP TO 300,000 GOURAUD-SHADED 25-PIXEL DEPTH-BUFFERED TRIANGLES/S.

PETER FLETCHER

Over the last few years, developments in graphics ICs have seen silicon devices that deliver greater performance for less cost. Still, unless price is no object, getting desktop 3D graphics capabilities generally requires a workstation that costs tens of thousands of dollars. Now one company, 3Dlabs Ltd. of Egham, England, claims to have made a major breakthrough with a single graphics chip called "GLiNT." The device reportedly will allow 3D graphics capability on a personal computer for about $1500.

The chip includes all of the functions needed to interface with a PCI bus *(Fig. 1)*. According to 3Dlabs' president and CEO, Osman Kent, "no glue logic is necessary to use GLiNT—just add memory and a RAMDAC." The device is purported to be a complete pixel production line, from rasterizer to video timing generator, all on one chip.

GLiNT is specified to compute graphics objects at a rate of up to 300,000 Gouraud-shaded, 25-pixel depth-buffered triangles/s. It will handle 750,000 24-bit, 10-pixel lines that are clipped, stencilled, and dithered each second, and will carry out 8-bit screen-to-screen copy operations at a rate of 48 million pixels/s. This means that with the chip's 50-MHz clock, GLiNT will run at around 2.5 billion operations/s. Target price for the chip is $150 in quantities of 50,000.

The chip is designed to run with a 3.3-V power supply with 3.3-V or 5-V signal levels available on all I/O pins. Power consumption is targeted at 3 W.

Although GLiNT was developed specifically for high-performance 3D graphics computation, its designers didn't neglect the 2D graphics required in a graphics user interface (GUI), such as X-Windows, Microsoft's Windows, Windows NT, and IBM's OS/2 operating systems. The chip's graphics processing core incorporates two independent pipelines, one for 3D and the other for 2D graphics.

"Our experience indicates that if 3D and 2D graphics processing are combined while heavy 3D processing is going on, all other operations are stopped, preventing the user from moving windows." To avoid that, the chip includes a hardware assist, so the 2D graphics operations can totally preempt the 3D functions by bypassing them, providing direct access from the PCI bus to the frame-buffer or local-buffer memory. As a GUI accelerator, GLiNT achieves a performance of 100 million Winmarks/s without impinging on 3D performance.

3Dlabs also has taken great care to ensure that GLiNT will be as easy to use as it will be to build into systems. The device was designed from the outset to provide an applications-programming interface (API) to the Open Graphics Library (OGL) developed by Silicon Graphics. In its simulated form, GLiNT has already tested positive against Silicon Graphics' OGL compliance suite of tests. But 3Dlabs stresses that while the company will use OGL as a benchmark, GLiNT isn't restricted to a single API. It can work with a number of other programming interface standards, such as that introduced by Intel Corp.

At the heart of GLiNT is a pipeline with 14 functional modules, each of which carries out a particular set of operations on the pixels passing along the pipe, very similar to a production line. Internally, all pixels are handled as full 32-bit pixels with full depth-buffering and a range of additional attributes, including antialiasing, alpha blending, and texture mapping. Only at the end of the line does a dithering unit adjust the information content of a pixel to match the display capabilities of its host system. Along the line, read and write access points are provided for local and frame-buffer memory. The interface between each stage is FIFO-buffered.

David Baldwin, chief consultant and project team leader, explains that along its length, the pipeline ranges in width from 32 bits to a full 64 bits. A high degree of parallelism is incorporated into the functional blocks. Because each block works independently of the others, up to 14 pixels can be in the pipeline at any time, for a 14-times performance increase.

System partitioning was developed to achieve maximum throughput along the pipeline, based on the company's experience designing 3D graphics boards for Sun workstations. It also means that each functional block can be adapted to meet new requirements as they arise. For example, there will be two versions of GLiNT when it's launched—GLiNT 300SX and GLiNT 300TX. They differ in the complexity of their texture-mapping abilities, a difference achieved simply by changing one of the functional blocks in the pipeline.

GLiNT's partitioning of the function blocks and their sequence along the pipeline is crafted in order to optimize processing time. This is achieved by filtering compute-intensive pixel operations that aren't needed, and allowing pixels to bypass processes that aren't applicable to them. For example, at the first stage after rasterization, a pixel is defined as belonging to an object that's behind another object; thus, it doesn't need to be displayed. As a result, some calculations that would normally be applied further along the pipeline—such as texture mapping—need not be applied to it. "That can save up to 100 operations," says Baldwin.

Along the pipeline, the first functional block is the rasterizer unit *(Fig. 2)*. It scan-converts a primitive shape computed by the host system into a list of X-, Y- and Z-pixel coordinates, according to the rules of OGL, X, or Windows NT. It also performs pixel-coverage calculations, subsequently used for antialiasing.

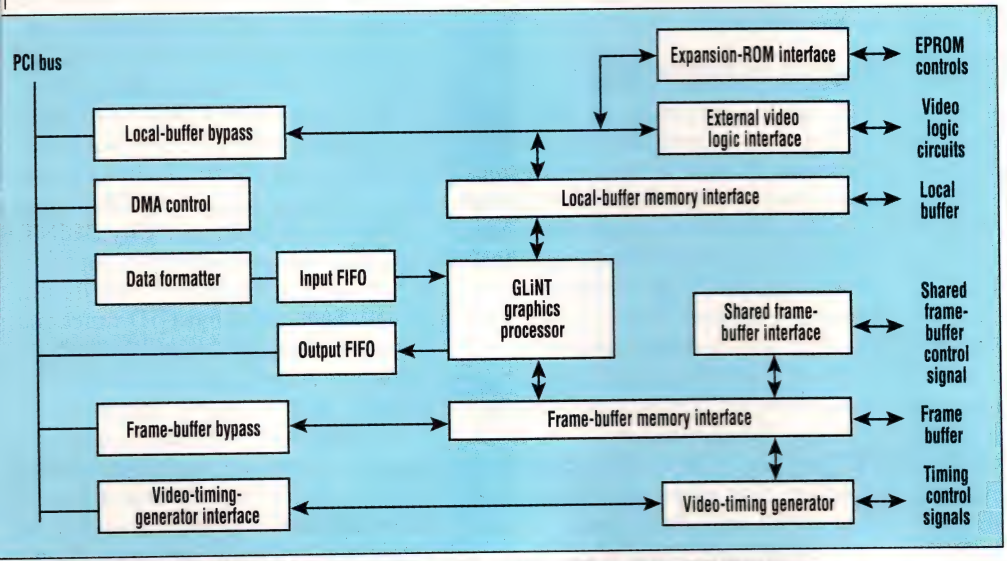
Next, the scissor-and-stipple unit filters pixels passed on from the rasterizer by performing four tests. These tests determine whether the pixel is within the boundaries of the screen, whether it falls within part of a window that's hidden or otherwise allocated to a forbidden area of the display, or if it falls under a stipple-masking pixel.

After that, a color digital differential analyzer (DDA) generates color information components of red, green, blue, and alpha. All four elements are generated in full, even though in some modes not all are required. If the chip is working in a flat-shading mode for 2D graphics to drive a GUI, then color values are taken from a constant color register and the pixel is forwarded along the line.

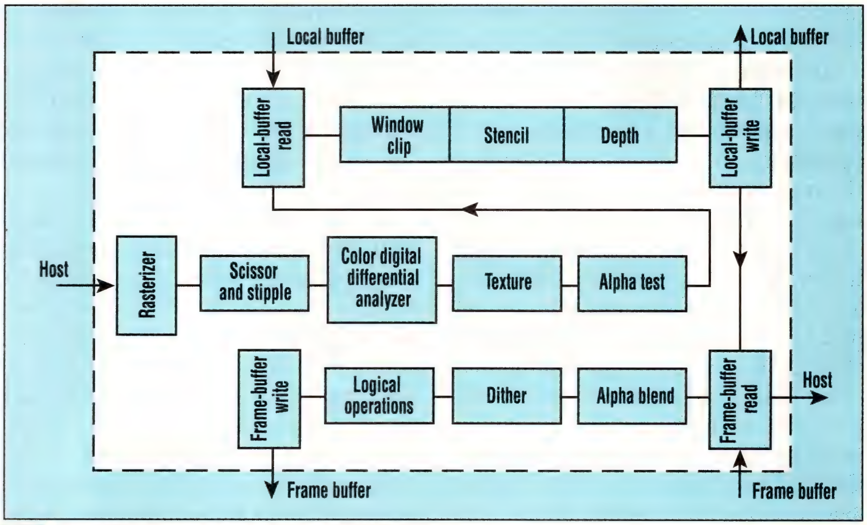
The following function, which also happens to be the most complex, applies texturing and what Baldwin calls "fog." This block differentiates the two versions of the chip—the GLiNT 300SX and TX. Both chips contain full implementations of the fog function, blending a user-defined background color with the pixel color to give an illusion of distance or additional depth cues.

The texture unit applies texture information derived from an externally stored texture map, up to 2 kpixels by 2 kpixels in size, onto the polygon's pixels. For the GLiNT 300SX, the texture unit implements the filtering necessary to reduce the aliasing artifacts. Up to 8 filtering modes are supported. The most sophisticated filtering mode, trilinear MIP mapping, requires 8 texture-pixels (texels) and 5 interpolation coefficients to be processed per pixel. Texture can be applied using three techniques: a decal mode, in which the texel color replaces the pixel color; a modulate mode, in which the texel color scales the pixel's color; and a blended mode, where a constant color based on the texel value is blended with that of the pixel.

For the TX version, the texture unit implements all of the texture modes specified in the OpenGL API, including full trilinear MIP mapping with full-perspective correction, based on information held in the local-buffer memory. The texture unit calculates the read address for the texture map



1. INTERFACING TO THE PCI BUS WILL BE SIMPLE with the GLiNT graphics chip from 3Dlabs. The device will provide 3D workstation-like graphics and reportedly will sell for $150 in large volumes.



2. THIS 3D GRAPHICS CHIP, **developed by 3Dlabs, represents a total graphics production line that's aimed at personal computers and video games. The chip's functions are arranged for optimum processing time.**

and dispatches read commands to a local-buffer interface unit. The information returned from the buffer then is used to calculate the final color for the pixel. This process can use up to four data elements per texel for red, green, blue, and alpha colors, and applies to decal, modulate, or blended modes. Also, a border definition for each texture map can be stored with the texture map, allowing the texture unit to wrap or clamp a texture across a surface. Otherwise, the border value can be derived from a constant border-value register. The TX texture unit supports nearest-neighbor, bilinear and trilinear interpolation, all with perspective correction.

Any pixel that survives this treatment then passes on to an alpha test unit, in which its alpha value is tested against a reference. Upon passing the test, it continues on. Otherwise, it's terminated. The alpha unit uses the coverage value calculated in the rasterizer to modify the pixel's color as part of the antialiasing calculations.

After the alpha unit, a local-buffer read unit calculates read and write addresses for the pixel as well as controls the local-buffer interface unit. Coordinates can be either screen or scene window relative. This unit converts X-Y coordinates to linear addresses to access local-buffer memory and is complemented by a local-buffer write unit that's set in the pipeline after the next processing block. The local-buffer write unit computes stencil, graphic-identity (GID), and depth functions to compare with values left in the local buffer by previous pixels passing that way. A fast clear mode is provided for fast window changing in applications like real-time animation.

For the final three graphics functions, information is required from a frame store containing data on the previously written pixels in a sequence. A frame buffer-read unit that supports multiple-buffer formats comes next along the line, after which an alpha blend unit merges a pixel's color with that currently held in its position on its plane. Next, a dithering unit converts signals from the internal 24-bit color into a format suited to the host hardware. It provides 8 RGB modes, including 8, 5, or 4 bits per color component; a 3:3:2 format for 8-bit RGB signals; and a 1:2:1 format for 4-bit RGB signals. Also, 4- and 8-bit color index modes are supported.

Finally, a logical operations unit performs write mask and logical operations between newly processed and existing pixels. It can perform all of the logical operations defined in the OGL specification, and carries out bitwise masking and logical operations on any incoming data. At the end of the line, a frame buffer-write unit passes information to a memory interface, and generates masks for video-RAM block-fill functions. In the event that a write to the frame-buffer store isn't required because it's been bypassed, the unit simply sends a cancel write command.

SYSTEM INTERFACING

GLiNT is designed to fit into a system such as a personal computer or workstations with as few extra components as possible. In addition to the graphics processor core, the chip contains circuits to interface directly with a host-bus system, as well as memory and video drivers. Initially, the host interface will be customized for Intel's PCI bus. This is specified for synchronous operation at up to 33 MHz and provides three functions—an input FIFO with a DMA controller, a bypass interface that gives direct access to local-buffer and frame-buffer stores, and a control and status interface.

The PCI interface is optimized for single-cycle transfers on the bus in both slave and master modes. When operating with its graphics-engine clock at 50 MHz and the PCI bus running at a full 33 MHz as a slave, GLiNT provides read and write access to its FIFO at up to 120 Mbytes/s. In the master mode using DMA read only, it achieves an access of 110 Mbytes/s. For PCI slave-bypass access to local and frame buffers, reading and writing data rates are 10 and 20 Mbytes/s, respectively. The PCI slave-control register reads back data from the GLiNT pipeline at up to 20 Mbytes/s.

The local buffer holds control planes, such as those for depth, stencil, graphics identity, and fast clear control, as well as texture maps. To keep board manufacturing costs low, it's configured to use conventional DRAM rather than fast static RAM. It can range in size from 0 to 48 Mbytes, although Baldwin says that memory sizes larger than 32 Mbytes may need external buffering. The local memory is driven directly by GLiNT, and can be up to 48-bits wide, supporting various field lengths for depth, stencil, fast clear, and GID functions up to the maximum bit width. Texture maps are stored in any remaining memory as 32-by-32-bit arrays.

For example, if a configuration supported a maximum resolution of 1280 by 1024 pixels with 24 bits of depth information, 4 bits of stencil, and 4 bits of fast clear information in an 8-Mbyte local buffer, then 3 Mbytes would be available for texture maps. Similarly, the frame-buffer interface can support 8-, 16-, or 32-bit RGBA (red, green, blue, and alpha) color-index frame buffers for resolutions ranging from standard VGA at 640 by 800 pixels to 2560 by 2048 pixels. Split transfer cycles allow the frame buffer to be addressed linearly.

The frame-buffer data bus can be either 32 or 64 bits wide, and the buffer can consist of up to 32 Mbytes. "Usually, this will be video RAM, but a DRAM buffer can also be implemented for low-cost systems using resolutions up to a standard VGA format," says Baldwin.

For video output, GLiNT contains an internal timing generator and a VRAM transfer controller that can be used in simple frame-buffer configurations. More complex configurations for stereoscopic, overlay, or interlace capabilities, or those that contain a frame buffer of more than 4 Mbytes, will require an external timing generator and transfer controller. Also, internal support is provided for lookup-table digital-to-analog converters (DACs) with 32-, 64-, or 128-bit pixel buses. Other types of lookup-table DACs may require external circuits.

The frame buffer's flexibility is key in making GLiNT suitable for the design and production of low-cost 3D graphics accelerators in PCs and video games. For example, the interface, when used with a 32-bit data bus, supports the shared buffer interface of the S3 graphics accelerator chip that's widely used in personal computers. The company claims that at least one potential customer is planning a board that will retail for less then $400.

In addition to shipping GLiNT as a ready-packaged device, 3Dlabs also plans to offer licenses for the chip's VHDL code. They will be offered to companies whose needs are best served by incorporating the 3D graphics core into circuits custom-made for a specific application, and in the longer term as an ASIC "megacell." For makers of board-level products, the company also will supply reference pc boards and full-design documentation, including board-layout Gerber tapes and device drivers, for at least three designs involving low-, medium- and high-functionality boards. The difference in functionality depends on how much memory a manufacturer wants to use to meet a target market price. ☐

PRICE AND AVAILABILITY

GLiNT 300SX and TX chips will be available in several formats—as chips, as VHDL source elements, or as ASIC megacells. First silicon is scheduled for August, with engineering samples expected in the last half of this year. Target price for the 304-pin QFP GLiNT 300 SX is estimated at $150 each in lots of 50,000. Prices for other formats and for reference-board design kits have yet to be announced.

3Dlabs Ltd., Meadlake Pl., Thorpe Lea Rd., Egham, Surrey, TW20 8HE, England. Telephone +44 (0)784 470 555.

3Dlabs Inc., 2010 N. First St., Suite 403, San Jose, CA 95131; (408) 436-3455.

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PRODUCTS NEWSLETTER

IMPROVED FPGAs BOOST DENSITY, SHRINK DELAYS

Providing a 20% speed upgrade of its XC3100 family, Xilinx Inc., San Jose Calif., has released the XC3100A-2. The enhanced chip can operate at interna speeds of up to 233 MHz for data paths, 180 MHz for 16-bit loadable prescaled counters, and deliver combinatorial delays of just 2.2 ns. To achieve the speed upgrade designers moved to a finer-line process, improved the routing resources, and also added a soft-startup feature that sets all outputs into a slew-limited mode upon power-up. This limits ground-bounce noise as all outputs simultaneously turn on. The 5000-gate XC3190A sells for $63.05 each in lots of 100 units. Upgrades of five other family members will be released later this year. *DB*

CIRCLE 900

TOOLS AFFORD FAST TCP/IP NETWORKING

San Diego-based XLNT Designs Inc. has created a suite of networking software packages called Stackware that incorporate common network protocols, such as TCP/IP, ARP, RARP, UDP, and ICMP, as well as applications like BOOTP, TFTP, and Telnet. Starting with Stackware Basic, developers incorporate the UDP, IP, ICMP, and ARP protocols into an embedded target. The BOOTP and TFTP applications supply automatic network configuration and connectivity. Using TCP and Telnet, developers can add remote operation. All components are in C source code. A license, including source code, documentation, and example implementations, goes for $9900. For more information, call (619) 487-9320; fax -9768; e-mail: stackware@xlnt.com. *SVT*

CIRCLE 901

DAC HIGHLIGHTS THE LATEST IN SYNTHESIS...

Advances in synthesis tools were among the many highlights at the Design Automation Conference (DAC) that took place last week in San Diego, Calif. A new version of the ASYL+ logic-synthesis software from Innovative Synthesis Technologies (IST), Danville, Calif., targets control-dominated designs. These types of designs are characterized by complex control, branching, and sequencing decisions. Typical control-dominated applications include telecommunications, robotics, and signal processing. For these control-oriented systems, ASYL+ accepts design entry as a state-chart graphical or VHDL-text input description. Textual VHDL specifications are entered as hierarchical RTL state descriptions, and graphical entry is done at the RTL level through the Speedchart option.

Speedchart uses the graphics to generate synthesizable VHDL. Regardless of the entry method, ASYL+ synthesizes a controller circuit using finite state machines (FSMs) and datapath elements. ASYL+ uses ROM generators to create the FSMs, unlike conventional synthesis tools that create state machines from standard-cell-based implementations. ROM generators deliver fast state machines with short critical-path delays that are close to ROM access times in length. To create the datapath elements, ASYL+ employs algorithms that call out special compilers and library macros. The ASYL+ synthesis solution for control-dominated designs was developed principally for gate-array and standard-cell ASICs, and supports a broad range of devices. It's available for both PCs and Unix workstations. Pricing starts at $10,000 on the PC, and $15,000 on Sun workstations. The Speedchart option goes for $16,500. For more information, call Peter Robinson at (510) 736-2302. *LM*

CIRCLE 902

...AND SHOWCASES WHAT'S NEW IN ESDA SOFTWARE

A good deal of the recent DAC news focused on electronic-system-design-automation (ESDA) software. For example, Version 2.0 of the flowHDL tool from Knowledge Based Silicon Corp. (KBS), Columbia, S.C., adds functionality that addresses key needs of the ESDA market. The flowHDL tool is a graphical-design-entry, verification, analysis, and automatic code-generation toolset. New features include library support of macro-function HDL descriptions for design reuse, an improved graphical user interface, extensive control-flow and datapath capability, support for modeling memory arrays, and enumerated data types. Version 2.0 of flowHDL comes with a choice of VHDL or Verilog output for simulation and synthesis, graphical editors, simulator, waveform display, and HDL macro-function library. It runs on HP, IBM, and Sun workstations. List price is set at $4995. For more information, call (803) 779-2504. *LM*

CIRCLE 903

MODELER HELPS DEVELOP AND TEST ATM CIRCUITS

The ATM Modeler is a software-protocol analyzer from Vantage Analysis Systems Inc., Fremont, Calif., that tests circuits developed for asynchronous-transfer-mode (ATM) networks. Accessible through the company's VHDL simulation environment, the ATM Modeler provides a customizable test environment capable of simulating ATM networks with up to 4000 end systems and a wide variety of network traffic. Each end system can be designated as connected to the ATM network via a private user-to-network interface, or it can be connected directly to another ATM end system. In addition, the traffic that's generated by the end system can be configured by specifying the number of call setups, duration of calls, quality of service, peak cell rate, and burst characteristics. During test and verification, VHDL circuit designers can still use the full debugging capabilities of the company's Optium VHDL environment. However, the ATM Modeler offers another level of verification by monitoring the performance and throughput of the total ATM network, as well as specific channels and datapaths. The ATM Modeler is available now for $40,000. Call Jim Cardwell at Vantage Analysis Systems Inc., (510) 659-0901 for additional information. *LM* **CIRCLE 904**

VHDL SIMULATOR RUNS FAST AT THE GATE LEVEL

Vulcan is a VHDL simulator from VEDA Design Automation, a Fareham, U.K.-based company that was spun off from the GenRad Design Automation Products Unit. The Vulcan simulator consists of a VHDL-1076 simulator kernel and compiler encapsulated within a series of user-interface tools. The kernel provides built-in primitives that map one-to-one to Vital primitives. This direct mapping allows Vulcan to accelerate Vital primitives, making the software both fast and accurate for submicron gate-level simulation. In addition, the Vulcan architecture has been designed to accommodate future developments, such as dual-timing simulation and fault simulation. The Motif-based user-interface tools include a source-level debugger, design browsers, and a waveform analyzer. Vulcan is available now for DEC, HP, and Sun workstations. Pricing is set at $20,000 for a single-user license. For more information, call Ray McNulty at (508) 263-2927, or contact the VEDA headquarters at +44 (0329) 822240. *LM* **CIRCLE 905**

HIGH-BRIGHTNESS LEDS CHALLENGE INCANDESCENTS

Designed to replace standard incandescent bulbs, the Q Series of high-brightness LEDs take advantage of the latest in LED-chip technology to produce high light output over a wide voltage range. The LEDs, from Data Display Products, El Segundo, Calif., are clustered in standard lamp-based packages, such as T-3-1/4 miniature, T-4-1/2 candelabra, or an intermediate size. The red lamp, based on an AlGaAs chip, offers a peak wavelength of 654 nm, a luminous intensity of 400 mcd at 20 mA, and a typical viewing angle of 40°. An amber version, which has an AlInGaP chip as its light source, peaks at 594 nm and provides brightness of 1000 mcd at 20 mA with a typical viewing angle of 30°. For the green LED, the chip is a GaP-on-GaP type. Brightness is 260 mcd at 20 mA with a viewing angle of 25°. All operate from voltages ranging from 5 to 110 V ac or dc or bipolar. The lamps are well suited for applications requiring ultra-bright, wide-angle illumination of switches, legends, and lenses in high ambient-light conditions. Pricing for the T-3-1/4 miniature bayonet Q Series lamp is $5.50 for red, $7.50 for amber, and $4.50 for green, all in quantities of 1000 units. Delivery is from four to six weeks. For further information, call the company at (800) 421-6815. *DM* **CIRCLE 906**

CLOCK OSCILLATOR HAS SMALL SMT FOOTPRINT

A fully integrated clock oscillator for surface-mount applications comprises an AT-cut crystal and all electronics needed to sustain oscillation, as well as wave-shaping circuits and low-impedance TTL outputs. The CO-2300 Series oscillators from Raltron Electronics Corp., Miami, Fla., require only 8.0 by 4.5 mm of board space with a low profile of 2.3 mm. They're enclosed in rugged resin-sealed ceramic packages with silver-lead contact pads on 2-mm centers. A glass insulator seals the package bottom. The oscillators need only +5 V for operation and consume a maximum of 30 to 75 mW, depending on frequency and fan-out. Outputs, which range from 2 to 40 MHz, are a 50% duty square wave capable of driving up to 10 TTL loads. Designs can be optimized by a choice of ±30-, ±50-, ±100-, or ±500-ppm accuracies at room temperature and of ±10-, ±30-, ±50-, or ±100-ppm stability over the full operating range of –10 to +60°C. Applications include portable products such as pocket modems, hard-disk drives, camcorders, and other high-density, surface-mount products. Pricing is from $2.60 to $4 in lots of 10,000. Parts are supplied on tape-and-reel for high-volume reflow-assembly operations. Delivery is in 10 weeks. For additional information, call Raltron at (305) 593-6033. *DM* **CIRCLE 907**

PRODUCTS NEWSLETTER

Socket Lets DX4 CPU Replace 486DX/DX2

The recently unveiled DX4 version of Intel's i486 CPU runs at three times, 2.5 times, or twice the external clock circuitry on a motherboard. Unfortunately, the DX4 cannot be used directly in existing i486DX/DX2 motherboards. That's because it requires 3.3 V, while the earlier, slower chips run from 5 V. But with the introduction of its upgrade socket and adapter (for the DX4 in 169-pin PGAs and 208-pin SQFPs, respectively), Aries Electronics Inc., Frenchtown, N.J., provides a quick, easy solution for motherboard upgrades. The socket and adapter contain the necessary circuitry to step down the 5-V voltage supplied by a DX/DX2 motherboard to the 3.3 V needed by the DX4 CPU. The model 57-U486DX2X upgrade socket for PGA packages allows placement of the DX4 chip into the socket provided as part of the upgrade module and requires no soldering. The 57-U486DX3X upgrade adapter for SQFPs allows the chip to be converted to a leaded PGA package by soldering the Intel package to the adapter, a service that Aries can provide. Pricing for either part is as low as $12.90 in lots of 5000 or more. For more information, call Aries at (908) 996-6841. *DM*

CIRCLE 908

Card Readers/Encoders Make Data Secure

A complete line of standard swipe and insertion card readers and motor-driven hybrid card readers/encoders is available for magnetic-stripe and IC cards. The reader/encoders, from Omron Electronics Inc., Schaumburg, Ill., include the models HSR and HNR swipe readers; models SCR, SPR, SFR-N, and SFR-J manual insertion readers; and models MMW, MKW, and MCR motor-driven card reader/encoders. The swipe and insertion readers have applications in bank ATMs, electronic-payment systems, access control, office automation, and others. The motor-driven reader/encoders add uses in vending machines, ticket issuance, and fuel-pump interfaces. Call Omron for pricing and other information at (800) 556-6766. *DM*

CIRCLE 909

SMT EMI Filters Address Telecom Needs

Suppression of unwanted electromagnetic interference in communications equipment and computers is performed by the EMIFIL line of surface-mounted EMI filters from Murata Electronics North America Inc., Smyrna, Ga. One product is the L-Chip inductor, which forms a coil, with the help of Murata's precision thin-film technology, to allow for higher performance, higher frequency operation, and lower losses. The inductor's tolerance is specified at ±2%. Other features of the EMIFIL products include standard EIA package sizes, low profiles, high-current capability, monolithic construction, and effectiveness over a wide frequency range. Product groups include SMT ferrites, SMT feed-through capacitors, leaded three-terminal filters, and others. Call Murata for pricing and other information at (404) 436-1300. *DM*

CIRCLE 910

Tester Uses PC To Check Cables

A PC-based tester performs continuity tests on most popular cables and adapters to check for proper operation and to isolate faults in less than 1 s. The CableEye tester incorporates a test fixture that connects to any MS-DOS PC through its serial port. The system was introduced by CAMI Research, Lexington, Mass. at Electro '94 in Boston. The internal wiring of complex cables or adapters are then shown in color with connector and pin numbers. As a result, users can quickly assess differences between null-modem, crossover, straight-through, and other cable types. The tester comes with menu-driven software that matches test cables with a database of more than 150 common cables for descriptive notes and supplier data. The CableEye costs $1495. For more information, call (617) 860-9137. *JN*

CIRCLE 911

Data Boards Need No Expansion Slots

Two 100-kHz data-acquisition boards for the OEM market, the 16-bit DaqBook/216/OEM and 12-bit DaqBook/112/OEM, measure only 8-by-7 in. and do not require an ISA-bus expansion slot. The data-acquisition boards can be connected to a DOS-based or Windows-based personal computer using a standard parallel port, a high-speed enhanced parallel port, or a PCMCIA connection. Unlike ISA-bus boards, which must be placed in proximity to the host computer, the new boards can be mounted anywhere that can be reached by a standard parallel port cable. The boards, which are powered by any 10-V to 20-V dc source, were introduced by IOtech Incorporated, Bedford Heights, Ohio, at Electro '94. Each board offers eight differential or 16 single-ended analog inputs, two 12-bit analog outputs, four digital inputs, four digital outputs, and one counter-timer. Boards can be connected to get 256 analog input channels, while maintaining their 10-µs channel-to-channel scan rate. Each data-acquisition board comes with DaqView2, an interactive setup and data logging application, and PostView, a related application that lets users scroll through multiple channels of previously acquired data. The DaqBook/216/OEM costs $995, and the DaqBook/

channels of previously acquired data. The DaqBook/216/OEM costs $995, and the DaqBook/112/OEM costs $1495 in single quantities. OEM discounts are available. Shipment is in two weeks. For more information, call Ron Gilbert at (216) 439-4091. *JN* **CIRCLE 912**

VXI CONTROLLERS RUN AT 100 MHZ

Based on the 100-MHz 80486 DX4 processor, the VXIpc-486 Model 599 offers users a PC-compatible controller for developing high-performance, VXI-based instrumentation systems. The Model 599 series includes one- and two-slot computers with 4 to 32 Mbytes of dual-port RAM and 256 kbytes (VGA), or 1 Mbyte (SVGA) of video RAM. The computers were introduced by National Instruments, Austin, Tex., at Electro '94. One-slot VXIpc-486 computers feature full PC/AT functionality with up to 220 Mbytes of hard-disk space. Two-slot models add a 3.5-in. floppy drive and have up to 525 Mbytes of hard-disk space. Both have connectors for an external floppy drive, a VGA or SVGA monitor, an IEEE-488 interface, serial and parallel ports, and VXI clock and trigger signals. An expansion kit for two 16-bit PC/AT plug-in boards is available for the two-slot models. The 486 DX4 is well-suited for VXI systems because the IC runs on 3.3 V dc rather than 5 V dc. As a result, the Model 599's power consumption and cooling airflow requirements are less than those of earlier models. The computers are compatible with all PC-based software tools. VXIpc-486 Model 599 prices start at $7495. For more information, call James Huron at (512) 794-0100. *JN* **CIRCLE 913**

DATA-ACQUISITION UNIT DOES MULTIPLE JOBS

The Model 8017 Precision Measurement and Data-Acquisition Unit combines the functionality of a multimeter, data-acquisition system, and data logger. The instrument, which is based on a 386 processor running under MS-DOS, features 80 input channels that can track such variables as ac and dc voltage and current, resistance, frequency, period duration, and temperature. The system was introduced at Electro '94 by Prema Precision Electronics, Montclair, Calif. A high-contrast LCD screen permits data to be displayed in numerical form or in a graphical x versus time diagram. Users can have the system perform statistical and mathematical functions directly on the graphical output of a measured value. Model 8017 prices start at $3600. For more information, contact Michael Merget at (909) 621-7292. *JN* **CIRCLE 914**

CD-ROM DRIVE CONNECTS WITH IDE INTERFACE

CD-ROM drives are typically built with SCSI or proprietary interfaces. Now, IDE interfaces are being used to connect the drive to the host system's motherboard, as in the CM207 drive from Philips LMS, Colorado Springs, Colo. The drive eliminates the need for a separate host-adapter card, reducing the system's cost. It also frees up a slot in the backplane as the drive will typically connect directly to the motherboard. The CM207 supports the IDE/ATAPI interface protocol. It features a double-speed data transfer, a 325-ms average access time, and a touch-sensitive, power-assisted tray-loading mechanism. The drive, which is compatible with the MPC 2 specification, includes a proprietary error-correction technology. The CM207 offers an MTBF of 30,000 hours. It is available now for $199. For more information, call Philips LMS at (719) 593-7900. *RN* **CIRCLE 915**

FLEXIBLE SWITCH CHIPS OFFER LOW COST

Featuring an infinitely programmable set of cross points, the IQ series of interconnect devices provides network product designers with the capability of up to 320 switchable connections on a single chip. Manufactured by I-Cube, Santa Clara, Calif., the IQ family is based on a proprietary switch technology that allows any point of the matrix to be connected to any other single or multiple set of points on the chip. The switch architecture is nonblocking, carries data at up to 100 MHz, and can be reconfigured dynamically at any time with a switching time of 20 ns. Each switch connection may be programmed to function as a straight or latched input or output, or even an auto-sensing bidirectional buffer. The programmable-switch family offers chips with 96, 128, 160, and 320 connections. At $0.20 to $0.30 per point, prices start at $19.60 for a 96-point switch in quantities of 10,000 units. For more information, call I-Cube at (408) 986-1629. *LG* **CIRCLE 916**

Edited by Clifford Meth

CALL FOR PAPERS

The Portable By Design Conference and Exposition

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Electronic Design is soliciting technical papers to be presented at the Portable By Design Conference February 15-17,1995 in the Santa Clara Convention Center, Santa Clara, Calif.

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Deadlines:

Abstracts: October 10,1994

Full Papers: December 1,1994

MOBITEX NETWORK FEATURES FLEXIBLE INTERFACE

Designed to meet the emerging needs of fixed data customers, the Universal Beta Unit, UBU, features easy connectivity to Mobitex networks from remote locations, interface flexibility, and the ability to accommodate many applications. Its powerful hardware/software interface, combined with a radio-modem on a single pc board, provide the means through which a remote user can control and monitor equipment at a substation. Information can then be transmitted to and from capacitor banks, automated switches, and reclosers.

At the heart of the UBU is an 8-bit microprocessor with 512 bytes of retentive memory and on-chip programming capabilities. An optional 32k-by-8-bit EPROM is also available. It is operated by a 12-V regulated dc power supply, over a temperature range of 0° to 70°. A number of convenient interfaces (including eight discrete inputs, eight discrete outputs, a programmable serial port, an a-d channel, and an opto-coupled input) are provided for interfacing to almost any device. Other features include an on-board received-signal-strength indicator, and dip switches to set common parameters. Also available is an optional RF switch, for use in applications requiring a redundant antenna system.

The UBUs design and flexibility provides a technology platform that allows for rapid, inexpensive development of applications, ranging from utility equipment to telemetry devices. It comes in a package that's 8-by-6-by-2.1 in., and weighs about 1 lb. Available now, the unit's cost depends on its specific configuration. CA

Cyplex, *472 Amherst St., Nashua, NH, 03063, (603) 882-8104.* **CIRCLE 620**

■ *CHERYL AJLUNI*

CELLULAR TRANSCEIVER CHIP SET SUPPORTS TDMA AND AMPS

A low-power integrated chip set performs all transmit and receive functions for both the new digital IS-54 time-division multiple access (TDMA) standard and the current analog (AMPS) standards for digital cellular phones. The four-chip set consists of the SA601 RF front end, the SA637 digital IF receiver, the SA7025 dual-frequency fractional-N synthesizer, and the SA900 I/Q transmit modulator.

Control of the transceiver is accomplished via serial interfaces to the synthesizer and modulator chips, which permit programming of operating frequencies, receiver gain, transmit power, or invoke a power-saving "sleep mode." The SA601 RF front end integrates an LNA and mixer to translate the received RF signal to a first IF. The IF receiver includes a mixer and oscillator with buffered output, two IF amplifiers, a fast logarithmic received strength indicator (RSSI), and voltage regulator. It performs demodulation of the incoming signal, providing analog phase and amplitude signals for processing by a DSP chip.

The RSSI output op-amp feedback pin is accessible, so designers can adjust output level or add filtering. The SA7025 advanced frequency synthesizer for the chip set features fractional-N division synthesis, providing selectable channel spacing of 10 to 5000 kHz. The synthesizer's rapid switching capability (less than 2 ms) meets the TDMA standard's strict frequency agility requirements. The SA900 dual-mode transmit modulator can operate as a conventional analog (AMPS) modulator or provide a complex I/Q signal for digital TDMA (IS-54) operation. Featuring an on-chip PLL synthesizer with VCO, the modulator also boasts a crystal oscillator buffer, programmable prescalers, and a Gilbert cell-multiplier phase detector with programmable charge pump output.

Operating at 3 V, the entire set draws only 90 ma while transmitting, and 30 ma in transmit mode. Selection of the switchable "sleep" mode further lowers power consumption to 3.4 ma. Designers can further extend battery life by using a variable duty cycle scheme to alternate standby operation between receive and sleep modes. Cost for the entire chip set is $30.00 in lots of 1,000.

Philips Semiconductors, *811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409.*

CIRCLE 621

■ *LEE GOLDBERG*

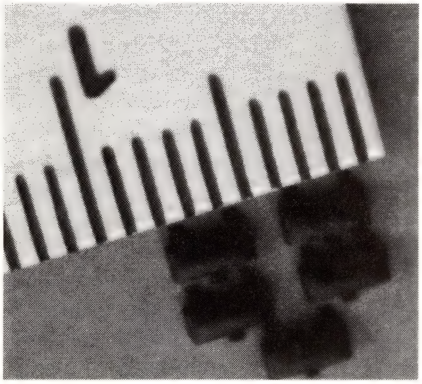
3V/5V ETHERNET COMBO IC HAS PCMCIA INTERFACE

The design of Ethernet interfaces for PCMCIA interfaces has been reduced to a single-chip solution by the 78Q8373 Ethernet Combo IC. Operating on either 3 or 5V, the 78Q8373 contains a complete 10Base-T Ethernet transceiver system and easily connects to any PCMCIA 2.1 compliant bus. If desired, the PCMCIA decoding logic may be bypassed for connection to other types of busses. The chip features three user-selectable power-saving modes - intelligent, standby, and shutdown which may be configured through internal registers to maximize power savings. Scheduled for full production in the second quarter of 1994, the transceiver will cost approximately $19 in quantities of 100. LG

Silicon Systems Inc, Myford Road, Tustin, CA 992680; (800) 624-8999, Ext.150. **CIRCLE 622**

Low-Cost References Come In Small Sizes

A family of precision voltage references, the LM4040 and LM4041, offer a combination of stability, precision, and low cost, all in one small package. Ideally suited for data-acquisition systems, process control, portable or cellular equipment, and other space-critical applications, the LM4040/41 boast a temperature drift curvature correction and a low dynamic impedance. Fully specified over the temperature range -40 to +85°C, the LM4040 comes in 2.5-, 4.09-, 5-, 8.192-, or 10-V fixed-output versions. The LM4041 comes in a 1.225-V fixed-output or an adjustable 1.24- to 10-V version. Both references are available in either a surface-mount, the SOT-23, or standard SO-8 and TO-92 packages. Available from stock, the LM4040/41 (±2% accuracy) sells for $0.80, and the LM4040/41 (±0.1% accuracy) sells for $1.95, both in lots of 100. CA



Micrel Semiconductor, 1849 Fortune Dr., San Jose, CA, 95131; Marvin Vander Kooi, (408) 944-0970. **CIRCLE 623**

Multiplexers Boast Extended Signal Range

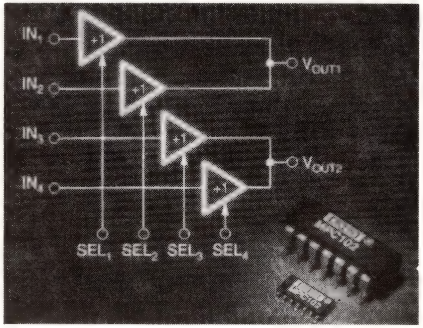
A series of four analog multiplexers, the AD408/409 and the AD428/429, feature an extended signal range, increased performance, and low cost. All four can be operated from single 5- to 12-V or dual ±15-V supplies over -40 to +85°C. With a maximum switching action of 150 ns, 1.6-mW maximum power consumption, typical on-resistance of 100 Ω, and a typical charge injection of 4 pC, the multiplexers are ideal for audio and video routing equipment, battery powered and portable computer peripherals, ATE, and communications systems.

During high-speed switching the ADG408/428 switch between eight single-ended channels, while the ADG409/429 switch between four differential input channels. The ADG428/429 also offer on-chip address and control latches to assure easy microprocessor interface. The AGD408/409 is available in a 16-pin plastic DIP, cerdip, or SOIC. In lots of 100, they cost $3.50 each. The ADG428/429 is available in an 18-pin plastic or cerdip package, or a 20-pin PLCC, with prices for 1000-unit lots starting at $3.15 each. CA

Analog Devices, Inc., 181 Ballardvale St., Wilmington, MA, 01887; (617) 937-1428. **CIRCLE 624**

Dual Multiplexer Suits Video Applications

A dual, 2-by-1 signal multiplexer, designed for wide-bandwidth systems such as HDTV and broadcast equipment, offers excellent harmonic and dynamic specifications. Its high data rate makes it equally well suited for other analog-signal-routing applications in radar, communications, and data-acquisition systems. The MPC102 is powered by ±5 V and operates over -40 to +85°C. It is composed of four monolithic open-loop buffer amplifiers, two of which are internally connected to create one output, with switching stages. Key specifications include a 210-MHz bandwidth, 640-V/μs slew rate, 68-dB channel crosstalk, and +6-mV/-8-mV switching transients. In addition, the MPC102 features ±4.6-mA (one channel) and ±230-μA (no channel) quiescent current, and differential gain and phase errors of 0.02% and 0.02°, respectively. The MPC102 comes in a 14-pin DIPs, SOICs, and dice formats. Demonstration boards are now available for test and evaluation. Production units are also available. In lots of 100, the MPC102 costs $7.41 each. CA



Burr-Brown, P.O. Box 11400, Tucson, AZ, 85734; Mary Douglass, (602) 746-1111. **CIRCLE 625**

Next-Generation Diode Optimized For Speed

The DFA25-10A HiPerFRED, a high-performance Fast Recovery Epitaxial Diode, is designed for use in power conversion and motor drive circuits. It is the first release in a family of next generation FREDs that were developed using a combination of silicon Schottky and PIN diode construction. The 29-A, 1000-V FRED is characterized by a fast switching speed, (30 ns), a guaranteed avalanche power rating of 13 kW, and a low leakage current of 20 μA. It also features excellent current characteristics and a soft recovery factor of one. Compared to to similar devices, the HiPerFRED also has 25% lower reverse recovery current characteristics. The DFA25-10A is available in TO-220, TO-247, and TO-264 packages. Future offerings from the HiPerFRED family will include 600- and 1200-V device versions in similar packages. Available now, the DFA25-10A HiPerFRED costs $4.14 each in lots of 1000. CA

IXYS Corporation, 3540 Bassett St., Santa Clara, CA, 95054; Rich Fassler, (408) 982-0700. **CIRCLE 626**

Inexpensive DAC Features Low Power

The HI1171, an 8-bit, 40-MHz DAC is specifically optimized for low-power operation. It draws a maximum of 80 mW and provides current or voltage outputs with the addition of an external resistor. Used in digital television, image processing, PCMCIA cards, and wireless LANs, it features a differential linearity of less than 0.25 LSB (maximum), and an integral non-linearity of less than 1.3 LSB (maximum). Its typical glitch energy is 30 pV-s, and differential gain and phase are 1.2% and 0.5°, respectively. The HI1171 DAC comes in a 24-pin SOIC. The HI1171 is now in stock. It is available in quantities of 1000 units for $3.86 each. CA

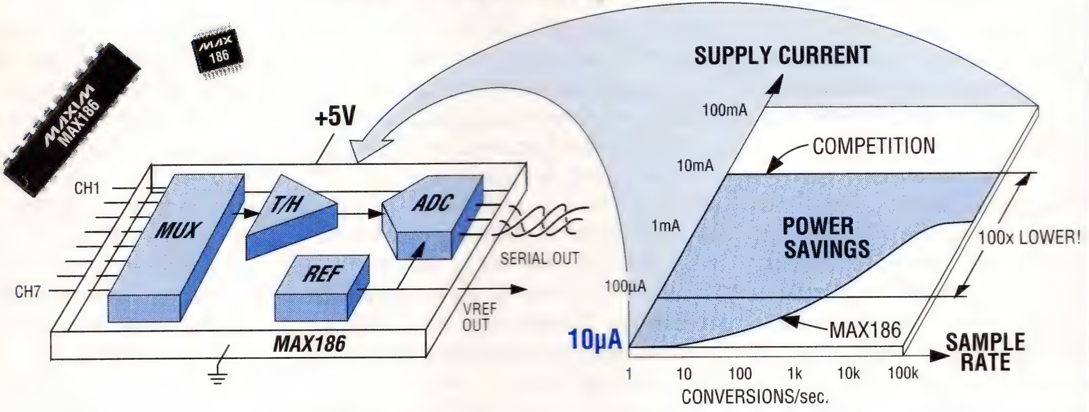
Harris Semiconductor, P.O. Box 883, Melbourne, Fl, 32901; 1-800-4-HARRIS, ext. 7138. **CIRCLE 627**

LOWEST POWER SERIAL 12-BIT ADCs DRAW 10µA AT 5V

100 Times Lower than the Next Best!

The MAX186/MAX188 A/D converters sample 8 single-ended or 4 differential inputs with a throughput rate as high as 133ksamples/sec. At lower rates, supply current drops below 10µA, including reference current! For single-channel applications the MAX187/MAX189 come in space-saving 8-pin packages.

Save Power & Space!



Choose Your 5V µPower 12-Bit ADC

Part #	Output Format	Input Channels	Ref	Sample Rate	Power Down (max)	Pins*	Price†	Call For EV Kit:
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MAX187	Serial	1	INT	75ksps	10µA	8	$7.45	MAX187EVSYS
MAX188	Serial	8	EXT	133ksps	10µA	20	$8.45	MAX186EVSYS
MAX189	Serial	1	EXT	75ksps	10µA	8	$6.95	MAX187EVSYS
MAX191	Parallel	1	INT	100ksps	50µA	24	$9.60	MAX191EVSYS

** Package Options Include DIP, SOIC, and SSOP*
† 1000-up Recommended Resale, FOB, USA

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READER SERVICE 217

FLEXCORE LIBRARY EASES THE TASK OF EMEDDED-CONTROLLER OPTIMIZATION

Even though many companies offer a selection of configuration options for their embedded controllers, it's a rare case when an off-the-shelf unit is a perfect fit for an application. For a better fit, designers often explore the possibility of creating an optimized version of the controller. But that process usually takes many months and is practical only for the highest-volume applications. However, with the FlexCore design library, designers at Motorola came up with a design approach that allows customers to create application-optimized versions of a controller quickly and with minimal design overheads.

Based on standard-cell design methodology, and dense, triple-level-metal cell designs, the FlexCore library allows designers to quickly bring highly integrated, yet application-optimized processors to market. Such processors can reduce board area and power consumption, yet at the same time improve system reliability and producibility. Designers would typically follow the production flow for a standard-cell chip—selecting and interconnecting the desired library cells, verifying the net list, and then fabricating the chip.

Custom products designed with the FlexCore scheme can include any of several 68000-family processor cores and 100,000 gates or more of custom (megacells or hand-crafted logic). Cores currently available include the 3 MIPS static EC000 and the 8 MIPS static 68020 processors. Additional cores now in development include a 12 MIPS 68030 (due late 1994), a 36 MIPS 68040 (due mid-1995), and 100 MIPS 68060 and PowerPC cores by late 1995. All the cores are updated and enhanced, but totally software compatible versions of the standard processors. The static-logic-based designs can operate at either 3.3 or 5 V, and allow the clock to be stopped to reduce power drain when no CPU activity is needed.

The FlexCore design approach combines Motorola's proprietary system design expertise and processor building blocks from the 68000 and PowerPC families. There will be two types of design "partnership" options offered by Motorola—for high-volume users, the relationship will allow the customer to craft a totally optimized solution starting with a 68000- or PowerPC-family CPU core. The alternative relationship would allow companies to design an optimized chip, but leverage Motorola's manufacturing and sales/distribution channel to market the product.

Companies that are using the first partnership approach include Digital Equipment Corp. and SunDisk Corp., which use the optimized controllers in the products it sells. The alternate approach, used by Peerless Systems Corp., allows Motorola to market the custom-designed controller in addition to Peerless employing it in its product. For developers, over 200 third-party tools already exist for 68000-based designs, and Orion Instruments Inc., Menlo Park, Calif., will support hardware emulation of the FlexCore elements. Because each process is a custom design, pricing varies, but a typical non-recurring engineering charge to support the design is about $125,000.

Motorola Inc., *Microprocessor and Memory Technology Group, 6501 William Cannon Dr. W., Austin, TX 78735-8598; Sue Cozart, (512) 891-2134.*

CIRCLE 628

■ *DAVE BURSKY*

MPEG I FULL-MOTION DECODER IC EASES MULTIMEDIA CARD DESIGN

In addition to performing full-motion-video decompression according to the MPEG I standard, the ZR36100 is the first MPEG I decoder to process the MPEG I system-layer information. That processing includes separating the discrete MPEG I video and audio bit streams and automatically synchronizing the decompressed video output with the output data of a downstream MPEG I audio chip. The ZR36100 decoder eliminates a considerable amount of system overhead logic, including the need for a host processor or dedicated microcontroller. That will further reduce the cost of adding MPEG I decompression to computer systems.

The CMOS chip fully conforms to the MPEG I standard, processing MPEG bit streams at rates of up to 5 Mbits/s. That allows the chip to support SIF resolutions for both 352-by-240-pixel NTSC (30 Hz), and 352-by-288-pixel PAL (25 Hz) formats. Features of the chip include user-selectable progressive or full CCIR601 interlaced video output, as well as special commands for 3:2 pull down, random access, fast search, slow motion, single stepping, and freeze-frame. In addition, the ZR36100 can do high-resolution still-image decoding.

The combination of features positions the chip well for cost-sensitive multimedia subsystems. As lower-cost systems proliferate, MPEG I playback will be adopted as a standard system feature, putting it in the mainstream, rather than relegating

VIDEO CHIP SUPPORTS AVI, MPEG ENVIRONMENTS

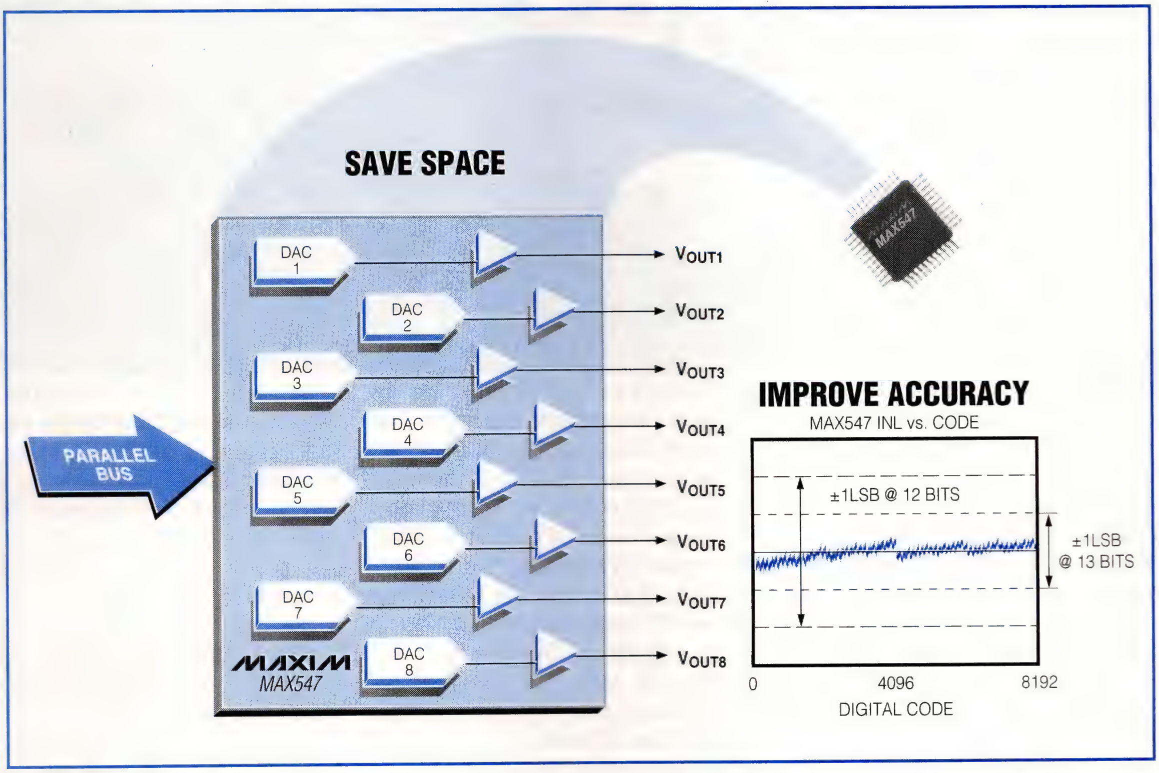
Designed specifically for Audio-Video Interleaves (AVI) and MPEG playback environments, the VxP201 video processor features full vertical and horizontal bilinear filtering. This includes scaling, zooming, anti-aliasing, and interpolation, all without the use of external line buffers or memory. Other features include a glueless interface to most popular MPEG audio and video decoders. On-chip audio-video synchronization support helps reduce the host overhead. High-resolution 24-bit true-color graphics are supported, up to 1280 by 1024 pixels. Samples of the VxP201 are available now. The VxP201 video processor is housed in a 208-pin plastic quad flat pack. RN

AuraVision Corp., 47865 Fremont Blvd., Fremont, CA 94538; (510) 440-7180. CIRCLE 630

REPLACE "8" 13-BIT DACs AND "8" AMPS WITH ONE IC!

Upgrade Your 12-Bit System to 13-Bits at Only $3.70/DAC*

The new MAX547 fits eight 13-bit DACs with output amplifiers in the space of one, while providing twice the resolution of 12-bit alternatives.



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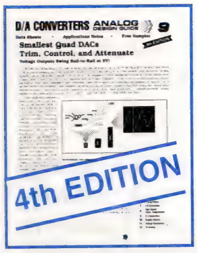
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READER SERVICE 218

TIMING CHIPS DELIVER HIGHEST SPEEDS, TIGHTEST SKEWS FOR TOP CPUS

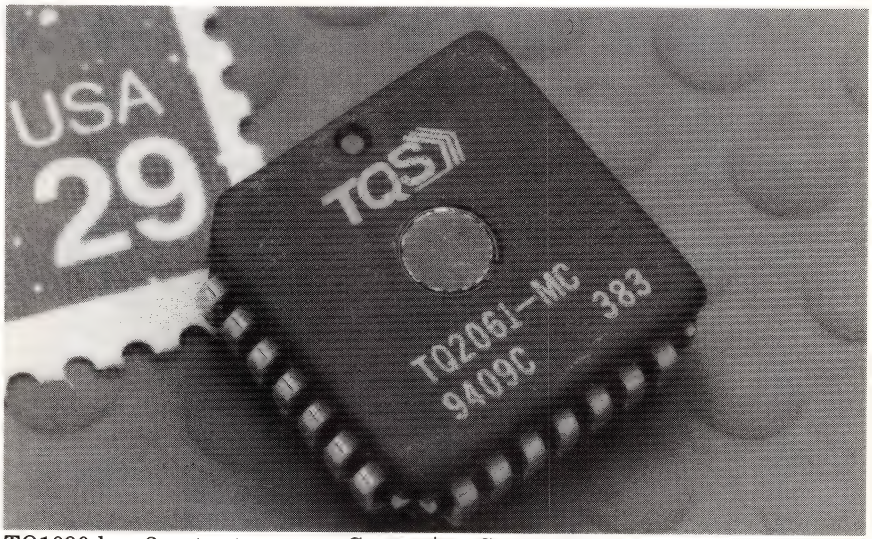
DAVE BURSKY

As the operating speeds of the most advanced microprocessors exceed several hundred megahertz, the clock buffers and generators that supply critical timing signals to the secondary cache memory, the CPU, and other subsystems play an important role in determining system performance. Large signal skews require that designers allow extra timing margins on the other components—that means either using more-expensive and faster parts to compensate for the larger skews, or reducing the skews and getting faster operation without upgrading system logic.

By keeping skews small—under 150 ps output-to-output within a group—TriQuint Semiconductor has come up with a moderately priced family of clock generators and buffers that are well suited for use with DEC's Alpha AXP, IBM and Motorola's PowerPC, and other high-speed CPUs. The family consists of the GA1089 and TQ1090, 11-output configurable clock buffers, and the TQ2059, TQ2060, and TQ2061 high-frequency clock generators.

The two clock-buffer chips are similar—both are in 28-lead J-leaded surface-mount packages and pack a phase detector, a VCO, division logic, and output buffers arranged in groups. The high-performance PLL formed by those blocks requires no external resistors or capacitors and operates with minimal jitter—under 200 ps period-to-period (worst case). Besides pin-to-pin skews of under 150 ps, the group-to-group skew on the same chip is less than 350 ps. Signal rise and fall time is 1.4 ns. Most of these numbers are at least 50%-100% better than other buffers.

Both chips can be configured in one of two output arrangements. The GA1089 has 8 outputs at the input reference frequency and 2 outputs at double the input. Or, it can be configured to deliver 9 outputs at half the input frequency and 1 output at the input. The 11th output is fed back to the input of the VCO. The TQ1090 has 3 output groups. Group A delivers 4 outputs at the reference frequency, 4 more at twice the reference from group B, and 2 more at four times the reference from group C. Or, it can deliver 5 outputs at half the reference frequency, 3 at the reference, and 2 at double the reference (A, B, and C, respectively).



Input reference frequencies can span 65 to 90 MHz for the GA1089, with outputs hitting 180 MHz on the high side. The TQ1090 allows for lower reference inputs. It accept 33 to 45 MHz inputs and still delivers 122 to 180 MHz on the 4X outputs. Higher-frequency versions will be offered—TriQuint expects 240-MHz options later this year. Both buffers offer near-zero propagation delays—350 ps ±500 ps, maximum (for more-relaxed systems, there are versions with a delay of 350 ps ±1000 ps).

With its abundant 1X outputs, the GA1089 is well suited for high-performance systems that typically operate at frequencies higher than the bus frequency. The TQ1090, with its mix of output options, fits well into moderate-performance systems that need both multiplied and divided clocks. The TQ1090 also allows the phase relationship of the group A outputs to the group B and C outputs to be varied by -2t, -t, 0, or +t (t = 1/VCO frequency). Both chips deliver symmetrical TTL-compatible signals and sink or source 30 mA.

Generating direct high-frequency clocks, the TQ2059/60/61 have output ranges of 200 to 350 MHz, 350 to 500 MHz, and 500 to 700 MHz, respectively, based on inputs of 20 to 35 MHz, 35 to 50 MHz, and 25 to 35 MHz. All three deliver one differential, positive-referenced ECL output with a 600-mV signal swing. Operating from 5 V, the clock generators have a common-mode voltage range of V_{dd} - 1.2 V maximum and V_{dd}dd - 1.6 V minimum. Period-to-period output jitter for the TQ2059 is 30 ps pk-pk, typical, and 120 ps, maximum. For the TQ2060, the numbers drop to 50 and 125 ps, respectively; while for the TQ2061, the jitter drops to 25 and 70 ps. Combined with the very tight low-jitter duty-cycle control, these devices meet the input specs for the Alpha AXP CPUs.

The clock chips also contain 200-Ω pull-down resistors that can be used when AC-coupled outputs are required. Several test modes are also included to simplify system debug and testing, by permitting the system to slow the clock or bypass the on-chip PLL. Samples of the clock buffer and clock generator chips are now available, with production quantities in the third quarter. Prices start at less then $9 in high volume.

TriQuint Semiconductor, 2300 Owen St., Santa Clara, CA 95054; Sunil Sanghavi, (408) 982-0900.

CIRCLE 631

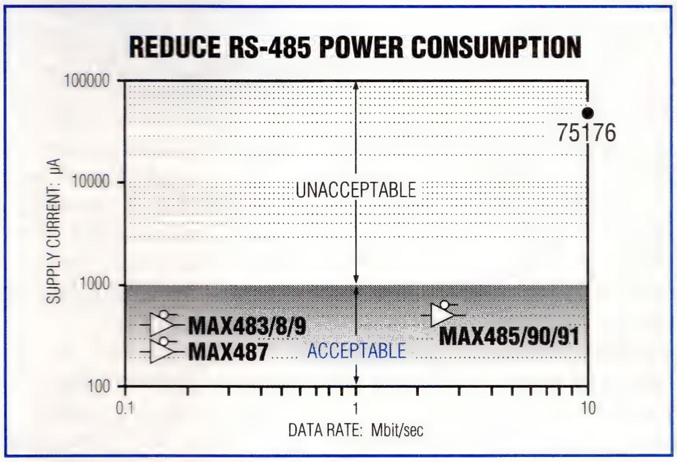
CUT RS-485 POWER CONSUMPTION IN HALF!

Lowest Power RS-485 IC Uses 250µA Supply Current—Max

The new MAX487 RS-485 transceiver uses a scant 250µA, making it the lowest power RS-485 IC available. The MAX487's ¼ unit load input impedance allows up to 128 transceivers on the bus at one time. Plus, slew-rate-limiting dramatically lowers radiated EMI while reducing reflections caused by mismatched cable terminations.

- ◆ **250µA Supply Current**
- ◆ **Full Duplex Available**
- ◆ **2.5Mbps Guaranteed Data Rate**
- ◆ **128 Transceivers on Bus**
- ◆ **1µA Shutdown Mode**

REDUCE RS-485 POWER CONSUMPTION



Specify the Optimum Low-Power RS-485 Transceiver for Your Design

	Part	#Tx/Rx	Data Rate Mbps	Max# on Bus	ISUPPLY (µA)	Full/Half Duplex	Price†	Feature
	MAX481	1/1	2.50	32	500	Half	$1.25	10µA Shutdown
	MAX483	1/1	0.15	32	350	Half	$1.25	Reduce EMI 100 Times
	MAX485	1/1	2.50	32	500	Half	$1.25	LTC485 Second Source
NEW	**MAX487**	**1/1**	**0.15**	**128**	**250**	**Half**	**$1.25**	**250µA ISUPPLY 128 MAX487s on Bus**
NEW	**MAX488**	**1/1**	**0.15**	**32**	**250**	**Full**	**$1.25**	**8-pin SO**
NEW	**MAX489**	**1/1**	**0.15**	**32**	**250**	**Full**	**$1.25**	**Separate Tx/Rx Enable**
NEW	**MAX490**	**1/1**	**2.50**	**32**	**500**	**Full**	**$1.25**	**LTC490 Second Source**
NEW	**MAX491**	**1/1**	**2.50**	**32**	**500**	**Full**	**$1.25**	**LTC491 Second Source**

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SCALABLE ARCHITECTURE GIVES LOGIC ANALYZERS EXPANSION CAPABILITY

The TLA 510 and TLA 520 logic analyzers use a scalable architecture called PowerFlex that allows users to extend acquisition memories as needed. The instruments come with 8-kbit-per-channel memories, which can be extended to 512 kbits/channel. In the timing mode, memory can reach 2 Mbits/channel.

The TLA 510 has 100 channels and can be expanded to 200 channels. The TLA 520 comes with either 150 or 200 channels. Microprocessor support packages are available for more than 100 devices, including the Intel Pentium and P54C. In the state mode, the units run at 100 MHz, and timing mode speed is 400 Msamples/s. A 16-state, 100-MHz, real-time trigger capability with two 32-bit counter-timers allows designers to accurately trace complex activity and locate sources of problems.

The graphical user interface is mouse-driven for easy operation, and a 14-in. color display speeds troubleshooting by display more information on the screen at once. Standard features include an Ethernet interface, so the analyzer can easily be integrated into an engineering network.

An optional performance analysis software package creates a graphical representation of where the user's software is spending most of its time. Consequently, designers can quickly determine where their time can most profitably be spent optimizing the program.

Base price for the TLA 510 is $18,000. Optional memory depths include 32 kbits, $4000; 128 kbits, $8000; and 512 kbits, $12,000. Base price for the TLA 520 is $33,000. Optional memories include 32 kbits, $8000; 128 kbits, $16,000; and 512 kbits, $24,000. The performance analysis software costs $1500. A 50-MHz pattern-generation option for the TLA 510 is $7290.

Tektronix Inc., *Test and Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200.* **CIRCLE 632**

■ *JOHN NOVELLINO*

VXI CARD EMULATES, TESTS COMPLEX BUSES

One two-slot VXI card holds both a bus-emulator architecture and stimulus-response architecture for testing complex digital buses. The SR192 offers up to 192 I/O channels and 20 timing and control signals. In bus-emulation mode, channels are grouped in 8-pin groups. In stimulus-response mode, each channel can be either an input or an output. Users can order channels in groups of 16 as needs change. Six SR192s can be synchronized to yield 1152 channels. Signals can be clocked at up to 50 MHz. Users can select TTL-compatible driver/receivers or driver/receivers that can be programmed to ±15 V with 50-mV resolution. Optional built-in DACs offer three voltage groups. The message-based module is compatible with the Standard Commands for Programmable Instruments. SR192 prices range from about $10,000 to $40,000 depending on channel count and options selected. Delivery is in 90 days. JN

Talon Instruments, 150 E. Arrow Hwy., San Dimas, CA 91773; (909) 599-0690. **CIRCLE 633**

PC-BASED SYNTHESIZER OFFERS HIGH RESOLUTION

Using 32-bit direct digital synthesis technology, the DDS-100 IBM PC/AT plug-in board produces sine waves from 20 Hz to 20 MHz with a resolution of 0.0116 Hz. The 10-bit amplitude is programmable to a jumper-selected maximum of ±1 or ±5 V. The unit can also supply a TTL-compatible square wave, which is generated directly from the sine wave and can be used to synchronize external equipment to the DDS-100. The board can serve as a programmable digital clock source because its TTL output has the same frequency range and resolution as the sine wave output. The board comes with a Windows application that provides a user-friendly interface that supplies frequency and amplitude selection and modulation functions that include am, fsk, frequency hopping, and burst mode. Included are software drivers for C and a dynamic link library for software development under Windows. The DDS-100 costs $495. Reseller and OEM discounts are available. JN

Quatech, 662 Wolf Ledges Pkwy., Akron, OH 44311; (216) 434-3154. **CIRCLE 634**

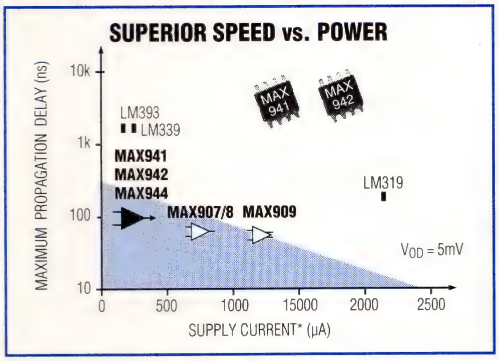
40-MHZ VXI COMPUTERS HOLD THE PRICE LINE

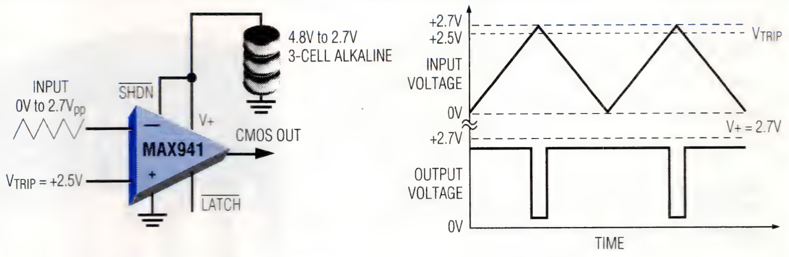
The VXIpc-486 Model 240 series of embedded VXIbus computers offers 40-MHz performance at the same price as the 20-MHz units they supersede. The C-size modules come in one-, two-, and three-slot versions. One-slot units feature full PC/AT functionality. Two-slot models add a 3.5-in. floppy drive and up to 525 Mbytes of hard-disk storage. The three-slot computers come with the 3.5-in. drive and up to 1.2 Gbytes of hard-disk space. All have connectors for an external floppy drive, a VGA or SVGA monitor, a GPIB interface, serial and parallel ports, and VXI clock and trigger signals. An ISA expansion kit for two 16-bit plug-in boards is available for the two- and three-slot computers. The computers use the proprietary TIC ASIC, which implements all VXI-defined protocols and features an internal cross-matrix switching system for routing between lines, as well as to and from the front panel and outboard clocks. The VXIpc-486 Model 240 is available now at prices starting at $3695. JN

National Instruments Corp., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. **CIRCLE 635**

INDUSTRY'S FIRST RAIL-TO-RAIL, 100ns COMPARATORS OPERATE DOWN TO 2.7V!

Input Range Extends Beyond the Supply Rails, Only 350µA Supply Current





With inputs that extend **beyond** the supplies, these devices compare signals as large as the supply without power-consuming resistor dividers.

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- **12µA Shutdown Mode (MAX941)**
- **No External Pull-Ups Required**

The new MAX941 single, MAX942 dual, and MAX944 quad are the first high-speed, low-power comparators guaranteed to operate from a 2.7V single-supply with a propagation delay of less than 100ns. And to simplify 3V and 5V designs even further, inputs extend **beyond** both supply rails, and outputs are CMOS/TTL compatible without external pull-ups.

Select the Ideal 3V or 5V High-Speed Comparator From the Industry Leader

PART	COMPARATORS PER PACKAGE	MAX. PROP DELAY (ns)	SUPPLY CURRENT* (µA)	MIN. SINGLE-SUPPLY VOLTAGE	INPUT VOLTAGE RANGE (V+ = 5V, V- = GND)	PRICE**
NEW MAX941†	Single	100	350 12(SHDN)	2.7V	-200mV to 5.2V	$1.40
NEW MAX942	Dual	100	350	2.7V	-200mV to 5.2V	$1.50
NEW MAX944	Quad	100	350	2.7V	-200mV to 5.2V	$2.50
MAX907	Dual	50	700	5V	-200mV to 3.5V	$1.70
MAX908	Quad	50	700	5V	-200mV to 3.5V	$2.95
MAX909	Single	50	1200††	5V	-200mV to 3.5V	$1.50

*Supply Current is per comparator, T_A = 25°C
**1000-up recommended resale, FOB USA
†MAX941 available in April, 1994.
††MAX909 has complementary outputs

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READER SERVICE 220

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First we cut noise, distortion, settling time and power. Now...

Now we've made big cuts in prices too. Recent reductions in our op amp family averaged 25%, which means you get exceptional performance for your money. That applies to the newest additions to our low-noise, voltage-feedback op amp family too. For example:

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Our new CLC426 couples high gain-bandwidth and low noise with a fast 400V/µs slew rate and 16ns settling time (0.05%). You get low distortion and adjustable supply current too. It's priced right for applications like wideband low-noise integrators, input buffers for hi-resolution A/Ds and other signal-conditioning applications requiring the combination of speed, low noise, low distortion and low dc errors.

Dual high-BW, low-noise op amp for $2.75/amp*.

In a class by itself, the new CLC428 packs two unity gain stable,135MHz GBW op amps with 2.0nV/$\sqrt{Hz}$ voltage noise in the same package. This leading-edge device also features a fast 400V/µs slew rate and 16ns settling time to 0.05%. This dual op amp offers great performance for the price and is ideal for multichannel integrator applications such as state-variable filters.

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Phone 44 203 422958, Fax 44 203 422961

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READER SERVICE 198

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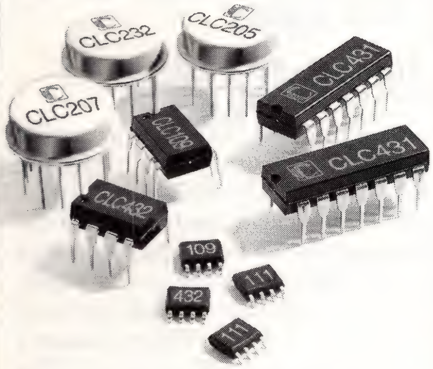
Bargain buffers and wideband op amps.



Fast buffers use little power. Pick from two new closed-loop, unity-gain buffers for video switch buffers, testpoint drivers and very high-speed active filters. The 270MHz CLC109 delivers a 350V/µs slew rate at just 3.5mA (± 5V). And just for $1.49*. The 800MHz CLC111 slews at a blazing 3500V/µs at 10.5mA. And it's only $2.75*.

READER SERVICE 200

Dual op amps also combine speed, low power. For dual selectable-gain amplifiers, video signal multiplexing and a host of amplifier and driver applications, pick the 62MHz CLC431(with disable input) or the CLC432. They take 7mA/Amp, slew at 2000V/µs, support video specs and operate on ±5 to ±15V supplies. Priced at just $2.99* and $2.49* respectively.

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Prices cut on ultra-high-performance hybrids. Need great distortion specs for fast, precision ADs and receiver IF stages? How about high output swing? Check the prices on our 170 MHz, high-gain CLC205 and CLC207. And the low gain, 270MHz CLC232. All three combine high speed with ultra low distortion. And prices start at just $24.50*.

*U.S. list price in 1,000s.

READER SERVICE 202

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SERIES OF TOOLS TEACH DESIGNERS BOUNDARY-SCAN TEST TECHNIQUES

Design and test engineers of nearly any experience level can increase their proficiency in IEEE-1149.1 (JTAG) boundary-scan test techniques with an array of training aids. The comprehensive collection includes a boundary-scan board, a videotape, a CD-ROM, training software, and two workshops.

The boundary-scan board was designed to evaluate IEEE-1149.1 test tools and equipment, as well as for educational purposes. The board has several boundary-scan devices, including an ASIC that supports built-in self-test, internal scan, and internal test. It also supports pseudo-random pattern generation, parallel signature analysis response capture, single and multiple scan paths, and interconnect testing.

The first part of the 74-min. videotape introduces design-for-test, the work of JTAG, and the IEEE-1149.1 specification. The second part goes more deeply into the specification, explaining the boundary-scan bus architecture and describing the benefits of testability.

The CD-ROM contains reference materials. Included is the IEEE-1149.1 standard, the Test Bus Evaluation Report, and applications notes and data sheets for Texas Instruments' catalog products. The report was compiled by TI's Defense Systems and Electronics Group to evaluate the effects of standard test buses on testability.

The Scan Educator training software, which is free, covers the fundamentals of boundary scan. The self-paced, menu-driven package runs on any IBM-compatible PC.

The two-day Design for Testability Workshop covers principles engineers should follow to design IEEE-1149.1-testable devices, printed-circuit boards, and systems. The Asset Workshop uses hands-on training with actual hardware to discuss TI's Advanced Support System for Emulation and Test.

The scan board costs $1295, the testability videotape $149, the IEEE-1149.1 CD-ROM $119, and the workshops $795 each per person. Workshop information can be obtained by calling (800) 336-5236 ext. 3904.

***Texas Instruments Inc.**, Semiconductor Group, SC-94033, Literature Fulfillment, P. O. Box 225558, Dallas, TX 75222-5558; (214) 638-0333.* **CIRCLE 636**

■ *JOHN NOVELLINO*

DIGITAL I/O CARD HAS 216 BUFFERED LINES

The PCDIO216-P buffered digital I/O board is useful for data acquisition, process control, and other applications that use TTL signals to drive indicator lights, 5-V contact closures, small relays, and other such devices. The PC/AT-bus board also supplies the high sink-current capability and pin-to-pin compatibility needed to interface with a variety of popular isolation relay racks. The board holds a total of 216 bidirectional, buffered digital I/O lines. The PCDIO216-P costs $425 and is available from stock to one week after receipt of an order. JN

Industrial Computer Source, 10180 Scripps Ranch Blvd., San Diego, CA 92131-1298; (800) 523-2320. **CIRCLE 637**

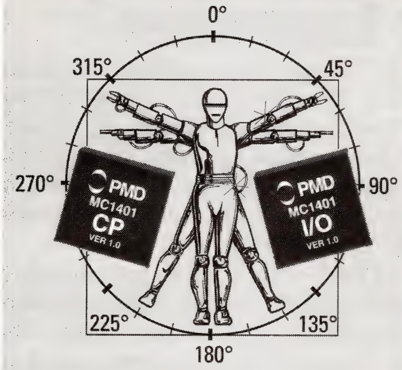
EMULATOR SUPPORTS 100-MHZ PENTIUM

The LA/ICE-I54 is an in-circuit emulator for Intel's Pentium processor at iCOMP index 815/100MHz (735/90MHz). The system supplies traditional emulation features like start-stop, examine-deposit, breakpoints, and single stepping. When combined with the ML4400 logic analyzer, the system offers real-time trace, trigger, and overlay memory. The emulator comes with a version of Systems and Software's SoftProbe protected-mode C debugger, which runs on the user's PC. Prices range from $10,000 for a debugging system without a logic analyzer to $34,475 for a fully equipped system. JN

American Arium, 14821 Chambers Rd., Tustin, CA 92680; (714) 731-1661. **CIRCLE 638**

Precision Motion

State-of-the-art Motion Processor



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Avoid months of design, testing and integration. PMD's new MC1401 already contains all the features you need at an incredibly low price.

The MC1401 interfaces directly to your motors and amplifiers. Designed into your system's control board–it's a complete motor controller on a chip.

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MC1401 Motion Processor Features

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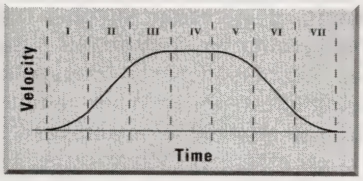

S-Curve profile increases smoothness and reduces load ringing, resulting in fast transfer times.

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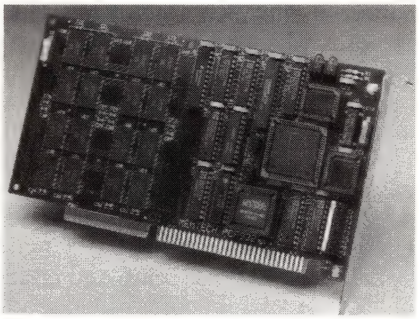
READER SERVICE 132

SOLID-STATE DISK DRIVE HOLDS 32 MBYTES

Up to 32 Mbytes of NAND EEPROM fit on the PCF932 solid-state disk drive. Compatible with the PC bus, the board is a rugged hard-disk emulator in an 8-in. XT card format. With no moving parts, it is highly resistant to dust, shock, and vibration. An operating temperature range of 0° to 70°C makes the board suitable for industrial-automation and process-control applications. Access time is rates at 0.5 ms, and sustained data throughput attains 6.4 Mbits/s. No device drivers are required—an on-board extended ROM BIOS allows it to run as a boot disk. The supply voltage is 5 V only, simplifying integration. Available now, the PCF932 sells for $2584 with 32 Mbytes, in quantities of 100. RN



MemTech Inc., 1257-A Tasman Dr., Sunnyvale, CA 94089; (408) 745-1600. **CIRCLE 639**

X.25 BOARD FITS 3U VME FORM FACTOR

The capability to handle X.25 communications is now available on a 3U VMEbus card. The VIX25 dual-channel card lets any VMEbus system implement long-distance digital communications over packet-switched public and private wide-area networks. It's built with a 16-MHz 68302 processor and holds 1 Mbyte of static RAM with circular buffers. The data-transfer rate ranges up to 2 Mbits/s for private networks, and 64 kbits/s for public networks. While consuming just 3.5 W, the board offers two full-duplex X.21bis channels. Bundled software allows the board to run the X.25 protocols without host intervention. The software interface with the host is done through shared memory on the VMEbus. The VIX25 is compatible with most standard real-time operating systems. The board costs $2055 in small quantities. RN

PEP Modular Computers, 5010 East Shea Blvd., Suite C226, Scottsdale, AZ 85252; (602) 483-7100. **CIRCLE 640**

AUDIO-CARD FAMILY FEATURES 3D SOUND

Three-dimensional sound can be achieved without software programming by the 3D family of audio cards. The 16-bit boards are built using the wave-synthesis technique for sound reproduction. The 3D sound comes from a proprietary Sound Retrieval System technology. Other features include 20-voice FM synthesis. The three boards include the Pro 3D, the Premium 3D SCSI 2, the Premium 3D MCD, and the Professional Wave Table Upgrade. The Premium 3D SCSI 2, which comes with a 2.5-Mbyte/s SCSI-2 adapter, and the Premium 3D MCD are wave-table upgradable. The Pro 3D consists of a Premium 3D SCSI 2 card, but has the upgrade already installed. It starts at $199. RN

Media Vision, 47300 Bayside Pkwy., Fremont, CA 94538; (510) 770-8600. **CIRCLE 641**

14-COLOR LCD ENHANCES INDUSTRIAL COMPUTER

A large color VGA flat-panel display accompanies the industrial computer in the DisplayPac-Vista. The complete workstation is built with a 14-in. color TFT LCD, a 66-MHz 486DX microprocessor, a resistive touch screen, and up to 32 MBytes of DRAM. The system suits space-conscious machine-control and process environments. The entire unit draws about half the power of a comparably sized CRT. It comes in a 12.5-by-15.5-by-4.5-in. rugged metal open-frame panel mount, or a 19-in. rack-mount version. Both have bays available for a 1.44-Mbyte floppy drive, a 2.5-in. hard drive (capacity up to 500 Mbytes), or a dual-slot PCMCIA socket. Six expansion slots accept standard AT-bus add-in boards. A 33-MHz DisplayPac-Vista system, with 4 Mbytes of DRAM, sells for $7435 in large quantities. RN

Computer Dynamics Sales, 107 S. Main St., Greer, SC 29650; (803) 877-8700. **CIRCLE 642**

ALL FOR PAPERS

The Portable By Design Conference and Exposition

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Electronic Design is soliciting technical papers to be presented at the Portable By Design Conference February 15-17,1995 in the Santa Clara Convention Center, Santa Clara, Calif.

Engineers experience in designing portable electronic systems of all types are invited to share their expertise. The range of eligible design applications includes computing, communications, data-entry, navigation and instrumentation-in either vertical and horizontal markets.

Papers should emphasize problem solving and provide insights into specifying and designing portable systems.

General topics to be covered include: Microprocessors and microcontrollers;Power Sources and circuits;Power management techniques; Batteries; Connectivity(e.g. docking, public wired network and all wireless); Software(e.g. operating systems including proprietary OS and application development); Peripherals (e.g. PCMCIA, GPS, storage); Displays; Input devices; industrial, medical, and test equipment; and, System design considerations (e g accelerated product development, testing, size, ergonomics, packaging, and ruggedness)

To participate, respond to this call for papers by sending a one-paragraph abstract of a paper you would like to present. Papers should be oriented toward solving specific design problems.

Abstracts should be sent to: *Program Chair, Portable By Design* Conference, c/o Electronic Design Magazine, P.O. Box 821, Hasbrouck Heights, NJ 07604. Or, send by fax to (201) 393-0204.

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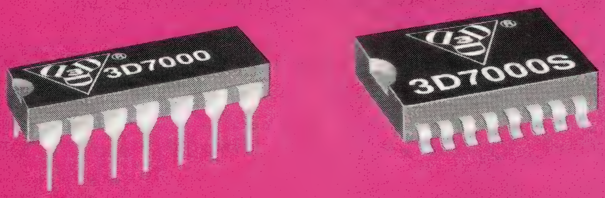

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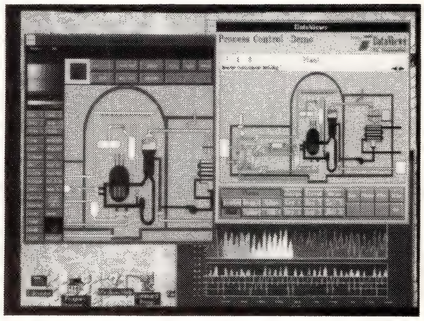
READER SERVICE 160

BUILD DYNAMIC DATA VIEWS UNDER WINDOWS

DataViews tools for dynamic data visualization now runs under Windows 3.1. With the software for Windows, developers can build customized animated graphics for visualizing, analyzing, and regulating live processes in real-time industrial, telecommunication, or scientific applications. Developers have a variety of graphics options to pick from; developing interfaces takes up to 80% less time. Also new is a developer's version of DataViews 9.5 on Microsoft Windows NT; DataViews 9.5 runs on 25 platforms and at least 20 operating systems. It supports the X Window System and is compatible with Motif. A development license for the Windows version is $11,000. Contact the company for other pricing. SVT



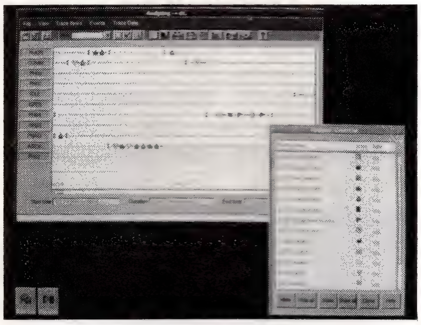
V. I. Corp., 47 Pleasant St., Northampton, MA 01060; (413) 586-4144; fax -3805. **CIRCLE 643**

TOOLKIT DEVELOPS DISTRIBUTED PROCESSING

The NetShare software development kit enables developers to incorporate distributed processing capabilities into their own software applications. Applications built with NetShare achieve performance gains and increased reliability by using an entire network of machines in parallel for task execution. Computer-intensive applications can be built to access NetShare, which monitors available network resources and matches them to application needs. The SDK is available for Sun, IBM, and HP platforms. Contact the company for pricing. SVT

Aggregate Computing Inc., 300 South Highway 169, Suite 400, Minneapolis, MN 55426; (612) 546-5579; fax -9485; e-mail: info@aggregate.com. **CIRCLE 644**

VISUAL SOFTWARE DEBUGGING TOOL SPEEDS EMBEDDED DEVELOPMENT



With the Embedded System profiler (ESp), developers of embedded applications can dynamically view and diagnose faults in complex multitasking applications. As a result, much of the guesswork of text-based debugging is eliminated. Through ESp's delivery of live images of pSOSystem application operations, developers can view the interplay of multiple tasks.

ESp graphically displays pSOSystem component configurations, memory stack usage and errors, kernel object inventories (tasks, semaphores, queues, regions, and partitions), user-specified events, and CPU use graphs. The main display supplies a dynamic view of context switches, task-state transition, interrupts, system calls, and all major application activities. Event-triggering and filtering capabilities let developers zero in on key performance parameters without being distracted by non-essential data.

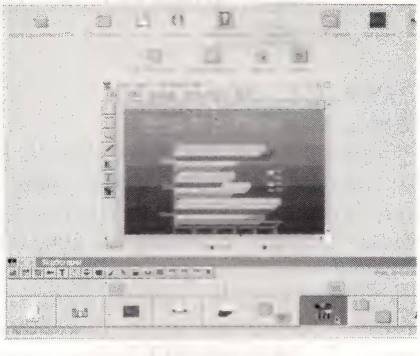
The ESp tool supports the company's pSOS+ and pSOS+m embedded real-time kernels. ESp software acts as a target-resident agent, collecting and relaying information about pSOS+ or pSOS+m kernel behavior over a networked or serial connection. The product's network connection affords board sharing among development team members.

The ESp network connection enables fault monitoring and diagnosis of systems in the field. Running on Sun workstations connected to Motorola 68xxx targets, ESp is scheduled to ship this summer. Prices begin at $4995; quantity discounts are available.

***Integrated Systems Inc.**, 3260 Jay St., Santa Clara, CA 95054-3309; (408) 980-1500; fax -0400.* **CIRCLE 645**

■ *SHERRIE VAN TYLE*

DESKTOP SUPPORTS OS/2 MULTITASKING



The SkyScraper Desktop Manager for OS/2 enables users to run or maximize many applications at the same time, each on its own desktop. Because applications are represented by a button in the manager's onscreen toolbar, users can switch between applications with a mouse click.

Users can launch programs and full-screen DOS sessions by dragging the program's icon to the SkyScraper toolbar and dropping it on any desk. Another feature simplifies daily system startup by memorizing how the desktop is arranged, and automatically restoring it each time the user starts up.

The toolbar is configured by the number of desks and their arrangement, or SkyScraper does it automatically. Applications can be shared among desktops for each access. Up to eight configurations can be saved to disk. System requirements are OS/2 2.0 or better; 386SX or above, 200 kbytes of hard-disk space; and 4 Mbytes of RAM. List price is $99.

***Binar Graphics Inc.**, 30 Mitchell Blvd., San Rafael, CA 94903-2034; (415) 491-1565; fax -1164.* **CIRCLE 646**

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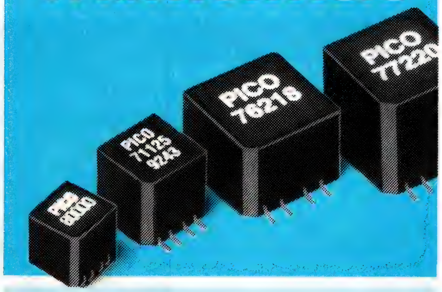

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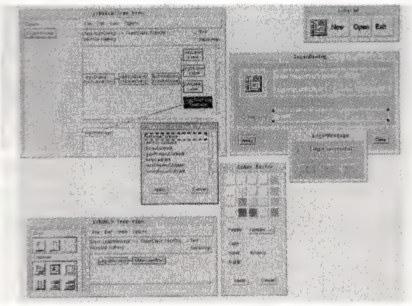
SOFTWARE TARGETS MOTIF GUI DEVELOPMENT

An object-oriented user interface design tool, iXbuild 3 eases programming in building Motif graphical user interfaces. Also available is a set of configuration file templates that let iXbuild users automatically generate interface code in the form of Rogue Wave View.h++ 1.2 C++ class libraries. Using the tool, developers can combine Motif widgets (self-contained packages of interface programming code) into graphical user-interface components, or classes, which are portable, reusable, and easily updated. GUI classes supply a higher level "building block" approach than Motif widgets, increasing programmer productivity and the quality of the interface code. The first user license is $4500. A product of iXOS Software GMbH, Munich, Germany, iXbuild 3 is available in the U.S. through Unipress Software. SVT



UniPress Software, 2025 Lincoln Hwy, Edison, NJ 08817; (800) 222-0550. **CIRCLE 647**

TOOL HELPS SHRINK TIME TO MARKET

Version 3.0 of the Energize Programming System is aimed at reducing development time on large software projects (upward of 500,000 lines of code). The system is an application development environment for C/C++ development on Unix systems. It supports full incremental development and supports code construction, maintenance, and reverse engineering of C and C++ code. The system includes the Lucid compiler and advanced editors, debuggers, and browsers to support the "edit-compile-debug" loop for programmers. With the system's shared database features, developers can work on a subset of a project without having to manage the entire project within their workspace, much like a configuration management system. Development teams can use read-only access to parts of their projects, reducing resource requirements while protecting the common base of code. Available at first on Solaris 2.x and SunOS 4.1, Energize 3.0 lists for $4250 for a single unit; upgrades to existing customers are free. SVT

Lucid Inc., 707 Laurel St., Menlo Park, CA 94025; (415) 329-8400; fax -8480. **CIRCLE 648**

MODEM SOFTWARE GAINS ENHANCED FAXING

QModemPro for Windows version 1.10 improves on its fax capabilities with the ability to launch data and fax communication from one dialing directory. The program supports RIPscrip from TeleGraphix Inc., of Huntington Beach, Calif., a de facto graphics standard for bulletin board systems (BBS). The upgrade eases sending faxes from QmodemPro by allowing users to configure the program as a print driver, enabling documents to be faxed directly from any Windows application. A user sends a fax with the Windows application's document print function and selects QmodemPro as the printer. List price is $139; free upgrades from Windows version 1.0 can be downloaded by dialing company headquarters BBS at (805) 873-2400. SVT

Mustang Software Inc., P. O. Box 2264, Bakersfield, CA 93303; (805) 873-2400; BBS (805) 873-2400; fax -2599. **CIRCLE 649**

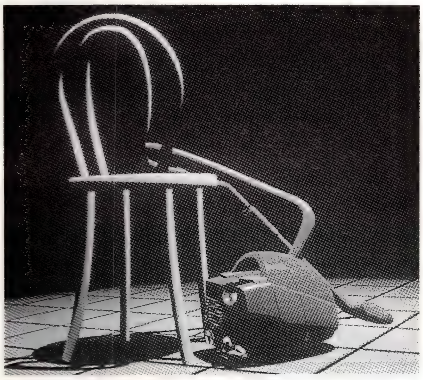
VISUAL SOFTWARE ANALYZES DATA

The Application Visualization System, AVS5, combines advanced data analysis and visualization capabilities for analyzing the large volumes of data generated by medical imaging, satellite-based sensors, and simulations. New to this version are support for ANSI C and C++ modules, direct user interface control for application development, a module source-code offering, and floating runtime licenses. It supports high-end graphics adapters. SVT

Advanced Visual Systems, 300 Fifth Ave., Waltham, MA 02154; (617)890-4300;fax-8287. **CIRCLE 663**

MINI SMT OSCILLATORS CUT INSTALLED COSTS

In addition to providing a wide range of output frequencies, the SMT S1600/S1650 oscillators feature plastic and ceramic packaging for lower manufacturing costs and improved end-product quality. The oscillators are available in frequencies from 1.5 to 80 MHz and are well suited for frequency generation and control in PCMCIA, telecom, instrumentation, and computer-system designs. Outputs are compatible with both HCMOS and TTL and can drive up to five TTL loads. The S1650 drives up to 50 pF and includes the tri-state function. Pricing ranges from $6.80 to $9 in lots of 100. DM



SaRonix, 151 Laura Lane, Palo Alto, CA 94303; (800) 227-8974. **CIRCLE 650**

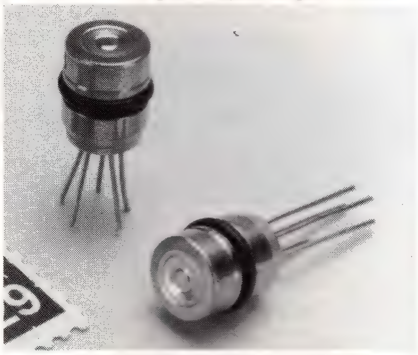
TOGGLE-SWITCH LINE GAINS QPL STATUS

C&K's line of miniature toggle switches has been qualified to the requirements of MIL-S-83731/09, /10, /13, /14, /15, and /16. Both single- and double-pole models are available with solder lug, straight pcb, and right-angle pcb terminations. Two actuator heights are offered with either a splashproof, threaded panel-seal bushing or an unthreaded bushing. All switches feature an epoxy terminal seal and are compatible with "bottom-wash" cleaning methods. Ratings are 5 A resistive, 2 A inductive, and 1 A lamp load at 28 V dc, 125 V ac (60 Hz), and 115 V ac (400 Hz). Pricing starts at $3.60 in lots of 500 with delivery in four to six weeks. DM

C&K Components Inc., 57 Stanley Ave., Watertown, MA 02172; Suzanne Lonergan, (617) 926-6400, ext. 8276. **CIRCLE 651**

MINI PRESSURE SENSOR HAS HIGH PERFORMANCE

An ultra-miniature pressure sensor, NPI-21A, has been optimized for easy integration into systems measuring gas or liquid pressures. It boasts a small, rugged, stainless-steel welded-package, high-reliability, and superior output stability, all for a low price. The NPI-21A sensor is offered in 0-3000 and 0-5000 psi ranges, providing typical nonlinearity of less than 0.1% full-scale output. In addition, the sensors have a typical full-scale unamplified output of 240 mV, and an output signal thermal accuracy of ±1%, operating over a temperature range of –10°C to +85°C. With a radial O-ring seal configuration, this sensor can be mounted onto pc boards. The NPI-21A pressure sensor is available in lots of 1000 for $25.50 each. CA



Lucas NovaSensor, 1055 Mission Ct., Fremont, CA, 94539; Bill Michaels, (510) 490-9100. **CIRCLE 652**

SUBMINIATURE FUSE WITHSTANDS WASHING

Measuring just 8 mm tall by 8.5 mm wide by 4 mm thick, the model TE5 subminiature fuse offers a footprint that's 25% of that of conventional glass-cartridge fuses and their clips. In addition, the TE5 fuse's pin spacing of 5.08 mm is half that of typical picofuses. The device is compatible with most automatic component-handling systems and withstands the rigors of wave soldering and board cleaning. Both fast-acting and time-delay versions are offered in current ratings from 50 mA to 6.3 A. Pricing starts at $0.30 each in OEM quantities. Delivery is in from eight to 10 weeks. DM

Wickmann USA Inc., 4100 Shirley Dr., Atlanta, GA 30336; (404) 699-7820. **CIRCLE 653**

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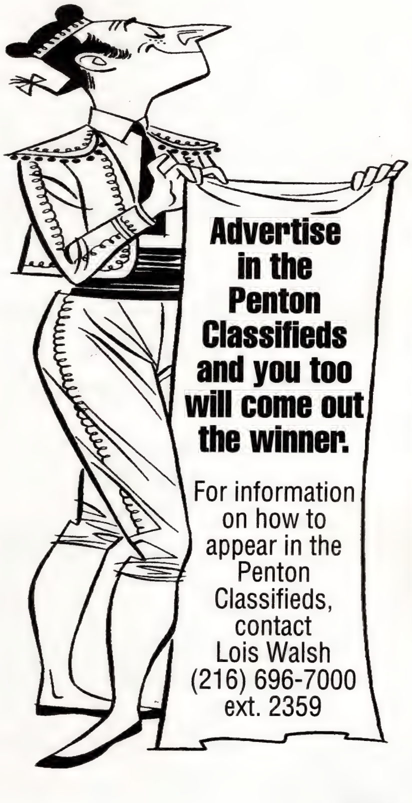
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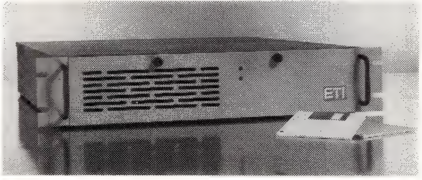
RACKMOUNT ENCLOSURES SAVE EQUIPMENT SPACE

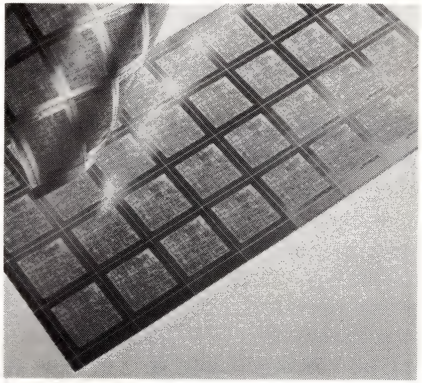
The same computing power can be designed into half the space of a conventional rackmount enclosure using the Series 4200 2U-high enclosures. Suited to telecommunication, industrial, and network-server applications, the enclosures can be built into consoles as well as mounted in 19-in. racks. Features include a six-slot modular passive backplane that accepts three full-length and three half-length 16-bit boards. The cards lay flat in a removable, T-shaped card cage that's the same height as a typical three-slot backplane. The model 4 205 is configured with a baby-AT motherboard and includes a five-slot card riser. Call for pricing and delivery. DM



Enclosure Technologies Inc., 256 Airport Industrial Dr., Ypsilanti, MI48198;(313)481-2200. **CIRCLE 654**

FLEX COMPOSITES ARE OF ALL-POLYIMIDE

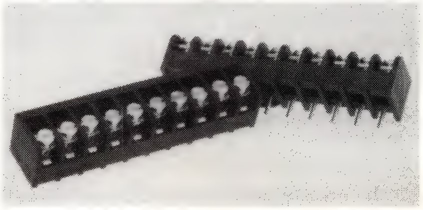
Military avionics, high-temperature sensors and probes, and under-the-hood automotive electronics are among the uses for the Pyralux AP family of all-polyimide flexible composites. The materials are designed to meet the needs for thinner, denser flexible circuits with higher signal speeds and improved thermal-management characteristics. The materials are particularly recommended for fabrication of double-sided, multilayer flex and rigid-flex circuits. First to be offered is double-sided copper-clad, which offers continuous thermal stability at temperatures above 200°C, excellent chemical resistance, and high peel strength. Call for pricing and delivery. DM



DuPont Co., Printed Circuit Materials, Barley Mill Plaza, Room G-52197, Wilmington, DE 19880-0010; (800) 237-4357. **CIRCLE 655**

TRI-BARRIER STRIPS HAVE 0.250-IN. SPACING

Designed to provide more circuits per square inch on limited pc-board space, the RSB2 Series of tri-barrier strips features 0.250-in. center-to-center contact spacing. The strips are UL-recognized at 10 A and 300 V. Their polypropylene insulator is rated at a UL flammability classification of 94V-0. Molded strips come with from two to 16 circuits, which can accept multiple wiring from 18 to 22 AWG under each Phil-slot clamping plate screw. The Phil-slot screws accept both Phillips and conventional screwdrivers. Price depends on quantity ordered. Call for more information. DM



Amerace Electronic Components, 7474 Utilities Rd., Punta Gorda, FL33982;(813)575-8400. **CIRCLE 656**

EPOXY ADHESIVE WON'T DETER HEAT

High thermal conductivity is featured in the Supreme 11AO electrically insulating epoxy adhesive. The material also offers a low thermal-expansion coefficient. Formulated to cure at room temperature or more rapidly at elevated temperatures, the adhesive has a convenient, non-critical 1:1 mix ratio by weight or volume. It can be applied without sagging or dripping even on vertical surfaces. Adhesion is excellent to metals, glass, ceramics, wood, vulcanized rubbers, and many plastics. Quantities range from pints to five gallons. Call for pricing and delivery information. DM

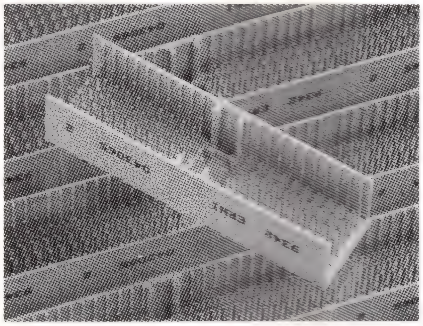
Master Bond Inc., 154 Hobart St., Hackensack, NJ 07601; (201) 343-8983. **CIRCLE 657**

HARD-METRIC 2-MM CONNECTOR MEETS HIGH-SPEED BUSING DEMANDS

The present and future demands of high-speed, high-density digital transmission systems are met by the ERmet 2-mm hard-metric connector system. Designed in compliance with IEC 917 and IEC 1076-4-101 standards, the system is well suited for applications requiring low crosstalk, controlled impedance, minimum reflections and propagation delays, and lower rise times. The system competes directly with Futurebus+ applications for 2-mm interconnects while offering mateability to products from other suppliers of 2-mm, hard-metric connectors.

Each ERmet connector module features five signal rows. There's also a five-plus-two version, the two extra rows being for shielding and grounding on a 2-mm centerline spacing. The units fit into 15-mm board spacing. Within the system, there are six basic board-to-board connectors in an inverse mating configuration. Among them are signal, high-current power, high-frequency coaxial, and fiber-optic connections that can be mixed and matched to form individually tailored connector systems.

For convenience in circuit design, the signal, hybrid power, and coaxial modular connectors are available in 50- and 25-mm modules for end-to-end stacking without contact loss. In addition, the geometry of the devices' female contact terminals assures virtually identical signal-propagation lengths and, therefore, identical propagation times.



Ruggedness is achieved through use of integral guiding and coding for optimum mechanical keying and polarization. For hot plugging and sequential staging of power, ground, and signal lines, the connectors offer three different contact levels. SMT compatibility is made possible through use of compliant pressfit terminals for both daughter-card and mother-board connectors.

Male modules are available from stock to six weeks, while female modules are scheduled for early summer release. Pricing will be announced at that time.

***ERNI Components Inc.**, 12701 N. Kingston Ave., Chester, VA 23831; (804) 530-5012.* **CIRCLE 658**

■ *DAVID MALINIAK*

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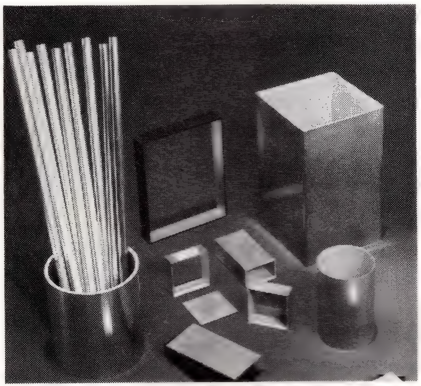
By laminating copper foil to the surface of fiberglass laminated polyimide tubes and headers, Stevens offers a solution to shielding of EMI and RFI at high temperatures. The printed-circuit-quality 1-oz copper foil is laminated to the tubing during the curing cycle. The material is rated for 240°C operation, meets UL-94V-1 flame requirements as well as MIL-P-13949F, resists shock and chemicals, and is machinable. Tubes and matching header plates are made to order from 4000 sizes of open-stock tubing. A 1-by-1-by-1-in. by 0.030-in.-thick tube goes for $2.45 and the matching header costs $1.50 each. DM



Stevens Products Inc., 128 N. Park St., East Orange, NJ 07019; (201) 672-2140. **CIRCLE 659**

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VERILOG DESIGN ENVIRONMENT MIXES COMPILED, INTERPRETED, AND XL SIMULATION ENGINES

SimLine is a Verilog simulation environment from FrontLine Design Automation that's aimed at complex-ASIC and large-FPGA designs. It combines compiled, interpreted, and XL simulation engines through a flexible, modular architecture. BaseLine is the company's low-end Verilog simulator targeted at programmable logic design.

The SimLine flexible architecture presents users with a unified, mixed-level solution. Central to this architecture is the Dynamic Model Switcher. With dynamic model switching, users can move quickly between the compiled, interpreted, and XL engines. This yields fast RTL performance, short turnaround for debugging, and fast gate-level simulation.

The Dynamic Model Switcher lets engineers combine different models and simulation engines as they progress through the various stages of the design cycle. In a mixed-level design, for example, the Switcher loads the RTL models into the compiled engine, and the gate-level models into the XL engine. Also, engineers modifying RTL code can avoid long compile times by invoking the interpreted engine for that particular RTL module.

DriveLine, another key feature of the SimLine architecture, synchronizes the various simulation engines and provides access to the simulation data structures. Because DriveLine is a single executable process optimized for language-based design, it delivers higher performance than does the conventional backplane synchronization approaches that are multi-process socket-based implementations. DriveLine separates functions such as hierarchy management, user-interface interaction, and PLI access routines.

SimLine features several new simulation capabilities that ensure timing accuracy and logic functionality for 0.5-μm technologies. For example, SimLine handles interconnects with multiple fanouts and drivers. And it models interconnect delays in both inertial and transport modes. The SimLine algorithms correctly simulate high-frequency designs, including simultaneous switching inputs and spikes where timing tolerances are very small.

The system's debugging and analysis environment was developed for HDL-based design from the start. Its graphical user interface includes a hierarchy manager, waveform- and register-display tools, and a source-level debugger. A design analyzer lets users examine the code, code coverage, and toggle count.

SimLine runs on Sun workstations, while BaseLine runs on both workstations and Windows-based PCs. Both products are available now. Pricing for SimLine starts at $27,500, which includes support for all three simulation engines. BaseLine pricing is set at $4995 for the personal computer and $9995 for workstations.

FrontLine Design Automation Inc., *2860 Zanker Rd., Suite 203, San Jose, CA 95134; (408) 456-0222.* **CIRCLE 660**

■ *LISA MALINIAK*

VHDL SIMULATOR ENHANCED WITH MULTIPROCESSING CAPABILITY

Vantage Analysis Systems has upgraded their VHDL-simulation offerings with a list of enhancements, including a multiprocessing simulation engine and ASIC sign-off capability. The company is also introducing a high-level transaction-based simulator.

SpeedWave/MT is a multiprocessing, multi-threaded VHDL simulation engine. The new engine runs on Sun Microsystems' Sparc10 multiprocessing workstations and servers, and delivers up to three times the speed of single-processor simulation engines.

Vantage is a member of the Vital VHDL-model effort, and is committed to supporting Vital sign-off simulation capability. They will bring the SpeedWave products to full Vital compliance in the third quarter. In addition, they will develop several new tools that make it easier for ASIC companies to create Vital-compliant sign-off simulation libraries.

Finally, Transaction Design (TD) Connection is a system-level analysis and modeling tool that's integrated with the company's VHDL simulation environment. Engineers can use graphical, icon-based Transaction Design models to verify VHDL descriptions. Systems are modeled with tokens and nodes.

All the tools run on Unix workstations. SpeedWave/MT will be available in the third quarter. TD Connection is shipping now. Call for pricing and additional information.

Vantage Analysis Systems Inc., *47211 Lakeview Blvd., Fremont, CA 94538; (510) 659-0901.* **CIRCLE 661**

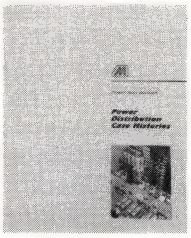
■ *LISA MALINIAK*

PC-BOARD TOOLS HAVE LOWER ENTRY PRICING

New product configurations lower the entry-price point for the Cooper and Chyan shape-based pc-board layout tools. With the release of Specctra version 5.0, the company will offer three low-priced base products for Unix workstations: Autoroute, Autoplace, and Editroute. These base products will be sold as individual tools or as part of a package. In addition to the Unix configurations, the shape-based autorouter is now also available as an entry-level PC-based product called SP2. SP2 offers the same algorithms used in the Unix autorouter, but is limited to two signal layers. Both the Unix and PC products are shipping now. Pricing for SP2 starts at $3750. Call for additional information. LM

Cooper and Chyan Technology Inc., 1601 Saratoga-Sunnyvale Rd., Suite 255, Cupertino, CA 95014; (408) 366-6966. **CIRCLE 662**

HISTORIES HELP POWER-BUS DESIGNERS



A rich source of ideas for the power-bus designer is found in an eight-page brochure with 30 power-distribution case histories. The brochure, from Methode Electronics's Power Buss Division, Rolling Meadows, Ill., borrows solutions from the computer and communications worlds and passes them along for application to problems with electronic and instrument interconnections. The company's custom bus bars offer simplified, error-free wiring at typically one-third the bulk of wire harnesses. Thirty or more insulation and conduction layers are laminated and bonded into a compact, sealed unit with any variety of accurately located mountings and termination nodes. DM **CIRCLE 670**

OPTOELECTRONICS CATALOG

The 1994 short-form optoelectronics catalog, from Siemens, Cupertino, Calif., is 88-pages thick—four-times larger than the last edition. The catalog features information on intelligent display devices, military high-rel displays, optocouplers, light-emitting diode (LED) lamps, infrared and fiber-optic emitters, and custom products. The catalog also contains information on Siemens product-quality programs. CM **CIRCLE 671**

RELAY DATA BOOK BRIMS WITH DETAIL

With over 430 pages, the Relay Technical Data Book from Aromat Corp., New Providence, N.J., is a valuable resource to any designer. This full-line catalog provides complete information on hundreds of relays of all kinds, including reeds, SSRs, optically isolated types, power relays, and more. A section of general technical information includes definitions of relay terms, diagrams of relay construction, general application guidelines, process information, and more. Individual products are described in close detail with tables of specifications and dimensional diagrams. DM **CIRCLE 672**

HIGH-POWER RESISTORS SUBJECT OF BROCHURE

Power handling from 10 to 800 W with values ranging from 0.5 to 20 kΩ is featured in a line of high-power resistors and terminations. The devices are the subject of a six-page brochure from RF Power Components Inc., Bohemia, N.Y. Included within the brochure are dimensional diagrams, technical information, and application notes. The resistors are wel suited for microstrip applications and feature low thermal resistance, low broadband VSWR and tolerances of 5% and 1%. DM **CIRCLE 673**

CATALOG OUTLINES BROAD SWITCH LINE

Basic snap-action switches, pushbuttons, slides, rockers, sealed types, and miniature pc-board switches are all contained within the standard switch product catalog from ITW Switches, Chicago, Ill. Complete product descriptions are prefaced by a section on switch terminology and diagrams of basic switch circuitry and movement characteristics. Each product is shown with dimensional diagrams and full explanations of mechanical and electrical characteristics. A part-number index rounds out the catalog. DM **CIRCLE 674**

PRECISION SWITCHES MEET SPECIAL NEEDS

A line of precision switches comes in sealed and unsealed versions, high-temperature types, and in typical assemblies, all of which are highlighted in a 16-page catalog from HSI Inc., Waterbury, Conn. Mechanical, electrical, and environmental characteristics are provided for all types. The catalog is profusely illustrated with photos and dimensional drawings. An overview of the company's capabilities, including custom designs, is included, as is a brief description of its testing and quality-control programs. DM **CIRCLE 675**

SUPPLY CATALOG COVERS WIDE RANGE

Detailed specifications, mechanical drawings, and prices for over 1000 standard power supplies, power systems, and accessories are contained in the 168 pages of the 1994 catalog from Lambda Electronics Inc., Melville, N.Y. Over 200 new products listed include the P Series high-density dc-dc converters, PFC Series multiple-output power-factor-corrected supplies, and FastRack ATE supplies. The latter features IEEE-488 programmability, fast response times, and low-noise outputs. DM **CIRCLE 676**

RF TASKS NOTED FOR 3-MM SWITCHES

A four-page application note from Bourns Inc., Trimpot Div., Riverside, Calif., describes how a 3-mm, SPDT rotary switch can be put to advantage in the design of RF circuitry. With numerous charts and graphs as well as a well-written short essay, it's shown how the model 7813 rotary switch can be used in RF circuits without causing signal distortion while handling signals at frequencies up to 1 GHz. Graphs illustrate such attributes as return losses, delays, and electrical isolation. DM **CIRCLE 677**

POWER-SYSTEM GUIDE AIDS IN SELECTION

One of the industry's broadest lines of distributed-power products is detailed in the 64-page 1994 Power Systems Selection Guide from AT&T Microelectronics, Mesquite, Texas. The full-color catalog covers supplies from the 2000-W RM Series front ends to 3- and 5-W board-mounted models. Sections detail AT&T's committment to quality as well as special features and application considerations. DM **CIRCLE 678**

ENCODED ROTARIES DETAILED IN CATALOG

A line of encoded rotary switches is fully described in a 16-page catalog from OakGrigsby, Sugar Grove, Ill. Two pages of general engineering information lead off the catalog, explaining subjects such as mounting methods, electrical data, torque requirements, lubrication, hardware, and more. Full electrical and mechanical specifications are provided for each member of the switch family. Dimensional drawings are included, as are tables of circuit codes. An application worksheet helps designers zero in on the right encoding for their circuit. DM **CIRCLE 679**

WORLD-POWER GUIDE UPDATES EXPORTERS

The line power available in countries around the world is listed in the Current Guide for World Power, a 34-page booklet from California Instruments, San Diego, Calif., that helps in correct testing of products for export. The guide illustrates the types of electric plugs for domestic and commercial use in most countries and lists each country's type and frequency of current, number of phases, nominal voltage, and number of wires. It also indicates whether the power is stable enough for electric clocks. Variances in major cities are also accounted for. A brief introduction highlights the company's single- and three-phase precision ac-power products. DM

CIRCLE 680

RELAYS, SWITCHES TARGET TELECOM

Relays, switches, and photomicrosensors for PBX, switching, transmission, and data-communication applications are covered in a 30-page catalog titled "Products for Telecommunications," from Omron Electronics Inc., Schaumburg, Ill. The catalog includes a selection guide and detailed specifications for individual products. An introductory section covers telecom-industry standards, UL flame retardancy, life testing, and component processing. A postpaid response card is enclosed. DM **CIRCLE 681**

BROCHURE HIGHLIGHTS TELECOM-POWER PLANT

The power needs of sophisticated cellular systems are addressed in a colorful 16-page brochure from Telecommunication Power Systems, Baltimore, Md. Among the highlights is a 1200-A cellular power plant that features a self-contained, space-efficient design. The modular system's distribution center handles up to 96 modular breaker positions to optimize system protection. The front-accessible system is available in either +24 V or –48 V dc in a 7-ft cabinet. Various system components are also described, including modular rectifiers, dc-dc converters, and a somewhat smaller version of the system. DM **CIRCLE 682**

MILLIONS OF OPTIONS FILL SWITCH CATALOG

Thanks to the Build-A-Switch format, Catalog No. 9308 from C&K Components Incorporated, Newton, Mass., gives users the opportunity to design their own application-specific switches from millions of possible option combinations. The 325-page catalog details a variety of switch types, including miniature, subminiature, and ultra-miniature toggles, rockers, lever handles, slides, rotaries, dual in-line packages, coded types, pushbuttons, piezoelectric, SMT, and process-compatible types. Complete specifications, including electrical and mechanical ratings, operating characteristics, and agency approvals are provided. DM

CIRCLE 683

BROAD POWER LINE MEETS MYRIAD NEEDS

New 100-W dual-output dc-dc converters, transformers, and inductors are features in Catalog #2023 from Pico Electronics Inc., Mt. Vernon, N.Y. The 136-page book introduces the P Series of high-power converters with a wide input from 18 to 380 V dc and output voltages from 3.3 to 100 V dc. The units offer dual isolated outputs with 100-W capacity. Also described are standard lines of thousands of transformers and inductors. An ac-dc power supply section offers linears and switchers in single, dual, and triple outputs. This series includes open-frame, encapsulated, industrial, and low-profile (0.500 in.) units. DM

CIRCLE 684

FILM RESISTORS IN VARIED ASSORTMENT

With 32 pages of engineering information and technical detail, a film-resistor catalog from Caddock Electronics Inc., Riverside, Calif., provides a valuable resource for designers. The complete scoop on a wide assortment of resistive elements is served up with tables of characteristics, descriptions, photographs, derating curves, and dimensional drawings. Included are high-voltage types, precision resitors, decade resistors, voltage dividers, shunts, resistor networks, power resistors, and more. DM **CIRCLE 685**

SOLUTIONS FOR PORTABLE APPLICATIONS

A 600-page data book from Benchmarq, Carrollton, Texas, describes Benchmarq's product focus in four categories. The first category, battery-management ICs, includes battery capacity monitors and single- and dual-battery fast charge ICs for battery-operated systems. The second category, real-time clock ICs and modules, includes modules that allow users to make inexpensive SRAM nonvolatile for EISA/MCA bus systems, portable PCs, and other applications. The third category is nonvolatile static and pseudo-static RAM modules, and the fourth category is nonvolatile controller ICs and modules. The free data book includes cross-reference guides and application notes. CM **CIRCLE 686**

PRODUCTS OFFER POWER PROTECTION

A 24-page, color catalog describes the power-protection products from EFI Electronics Corp., Salt Lake City, Utah. The long-form product catalog describes EFI's facility-wide solution to power and data-line protection from transient voltages and other power problems typically found in commercial, industrial, and medical facilities. In addition to in-depth product description, the company's product technologies are fully described. Included are model numbers for over 50 categories of power-protection products. CM

CIRCLE 687

INDUSTRIAL AUTOMATION CONTROL EQUIPMENT

Balluff Edition D, from Balluff Inc., Florence, Ky., describes many lines of control equipment for industrial automation. The 650-page catalog includes sections on each of the company's product lines. Balluff offers original equipment manufacturers and retrofit application users a wide range of proximity switches, optoelectronic switches, mechanical limit switches, rotary positioning switches, mechanical limit switches, rotary positioning switches, linear position devices, programmable limit switches, electronic identification systems, and motion control devices. CM

CIRCLE 688

ON RELIABILITY AND THE RADIOTRON BOOK

Your editorial of March 7, 1994 titled the Reliability Quest, really brought things home to me. I rely on the reliability of electronics daily, to live. On 17 March, 1989, I received a dual chamber pacemaker implant for a complete heart block. It works full time and on "demand," i.e., changes rates as needed. It works when the heart rate drops below about 120 beats per minute and stops working when the rate is between 125 and 148 beats per minute.

It is fascinating to note that the pacemaker can be programmed via a small unit that transmits and receives information on its condition right through the skin. Glad to have a reliable electronic instrument keeping me in good health and spirits.

In Readers' Comments, your answer to Mr. Whitman Reeve regarding the Radiotron Designer's Handbook was very good. I somehow missed the description in the column. I believe it was around 1575 pages, red cover, paper quite thin. My copies of the book are all gone. I used to buy them, sell them, and loan out my copy to other people who wanted to use it. My last copy was loaned to someone and never returned. It was a terrific book.

As Mr. Reeve indicated, it was very practical. The mathematical shortcuts in it were worth twice the price of the book. I think it was $7.00 from an electronics distributor in the late 60's. Mr. Reeve's description was quite adequate. I also think the book's short cuts allowed you to achieve approximately a 3-5% accuracy quickly, where you were using mostly 5 or 10% components. It helped me to think better and understand more.

A very good article, and very good comments.

CARL MERRILL
SOMERSET, MASS.

Editor's note: Regular readers may recall that in the March 7, 1994, Reader's Comments column, I recounted a bizarre occurrence related to my once owning a copy the Radiotron Designer's Handbook. I thought I still had my copy, until I received a note from Ideas for Design author Craig Merz, an engineer with ITI Manufacturing, Califon, N.J. The note enclosed a copy of the book's inside-cover page, which bore my name in my handwriting, and the date that I had bought it: 1-5-54. It seems that Craig borrowed the book from a friend, who had bought it in a used book store, and noticed my name in it. When we got to talking on the phone, Craig said that his friend was unlikely to let go of this copy unless he could find another one to replace it.

Now, to close out the story: I'm happy to report that Craig and his friend managed to find another copy of the book and have sent me my original. Here's Craig's note, which accompanied the book:

Dear Steve:

I hope this helps make your day. I didn't forget, it just took some time to locate another copy. That copy has the name: J.C. Prator, Jr. July 1955.

It's the fourth edition, a 1953 printing.

Seems like all the budding young engineers of the mid-fifties had a copy!

My thanks to Craig Merz for restoring to me this valuable contribution to the development of electronics technology.

Steve Scrupski
Editorial Director
Electronic Design Information Group

JEDEC TERMS CAN CUT ACRONYM EXPLOSION

Mike Peters' letter on acronyms in the Reader's Comment section in your March 7, 1994 issue strikes a familiar chord. At JEDEC, we develop package standards for semiconductors and other semiconductor device standards. In the early days of package standards, people used our reference numbers like TO-3, TO-5, TO-92 etc., to describe package types. However, in the 1980s, many industry people started using acronyms instead like LCC, SOT, SOG, SOP, and so on.

The problem with these is that they are vague and at times two different terms are used to describe the same thing. JEDEC still does use the reference numbers—I wish more people in industry did. A few examples are: MO-015 for DIP, MO-052 for PLCC, MO-143 for MQFP, TO-252 for DPACK.

JEDEC offers an index of package acronyms to JEDEC package outline drawings contained in JEDEC standards. If anyone would like one, contact us at the address below.

The acronym explosion has been amazing in size in the electronics industry. Our Terms and Definitions Committee recognized this problem some time ago and published a document called JEDEC Standard 30: "Descriptive Designation System for Semiconductor Device Packages."

The idea here was that it guided you on how to develop a new acronym that tells you something. The only problem is that these new acronyms are not catchy, and therefore may not be widely used. For instance, TSOP II becomes R-PDSO-G/TSOP II. The R means rectangular, P means plastic, SO means small outline, and G means gull-wing leads.

It may not be a perfect solution, but it's something.

Perhaps these acronyms are more cultural than anything. I remember a few years ago someone from a Japanese company recommended a new package type be called an SOB. Fortunately, some Americans talked him out of it, but it was funny.

KEN McGHEE
JEDEC SOLID STATE PRODUCTS
ENGINEERING COUNCIL
WASHINGTON, D.C.

Editor's note: To take Mr. McGhee up on his offer of a copy of the package acronym index, contact: JEDEC Solid State Products Engineering Council, 2001 Pennsylvania Ave., N.W., Washington, D.C. 20006; telephone: (202) 457-4971; fax: (202) 457-4985.

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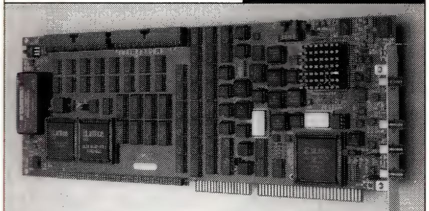

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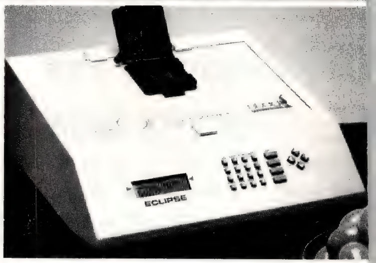

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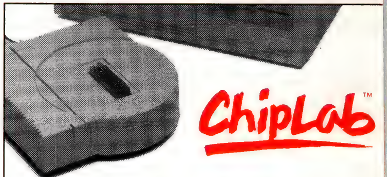

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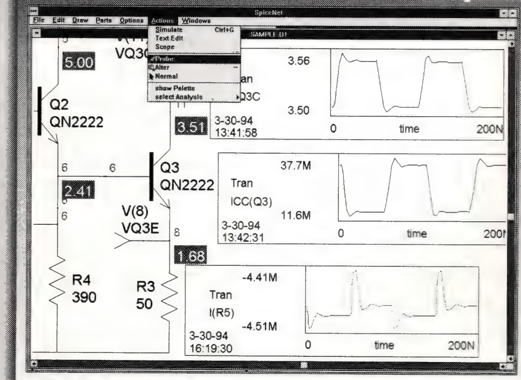

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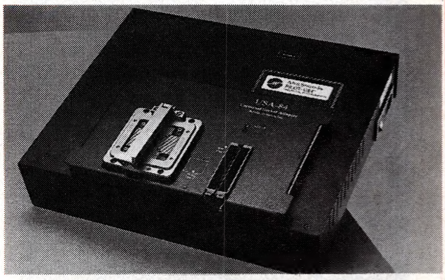

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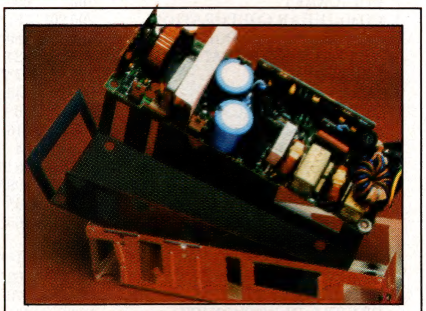

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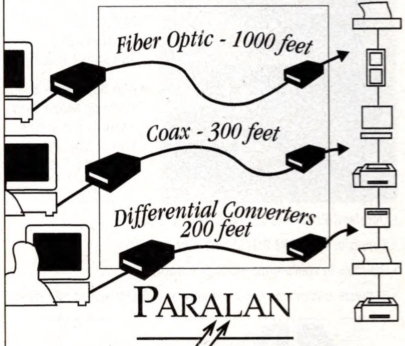

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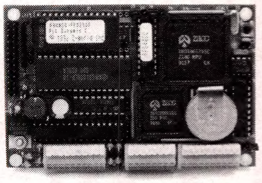

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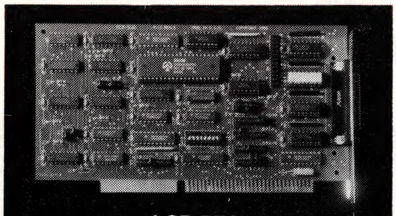

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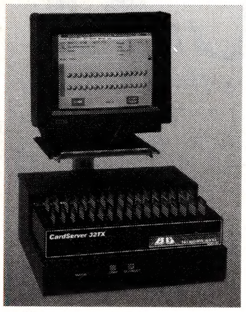

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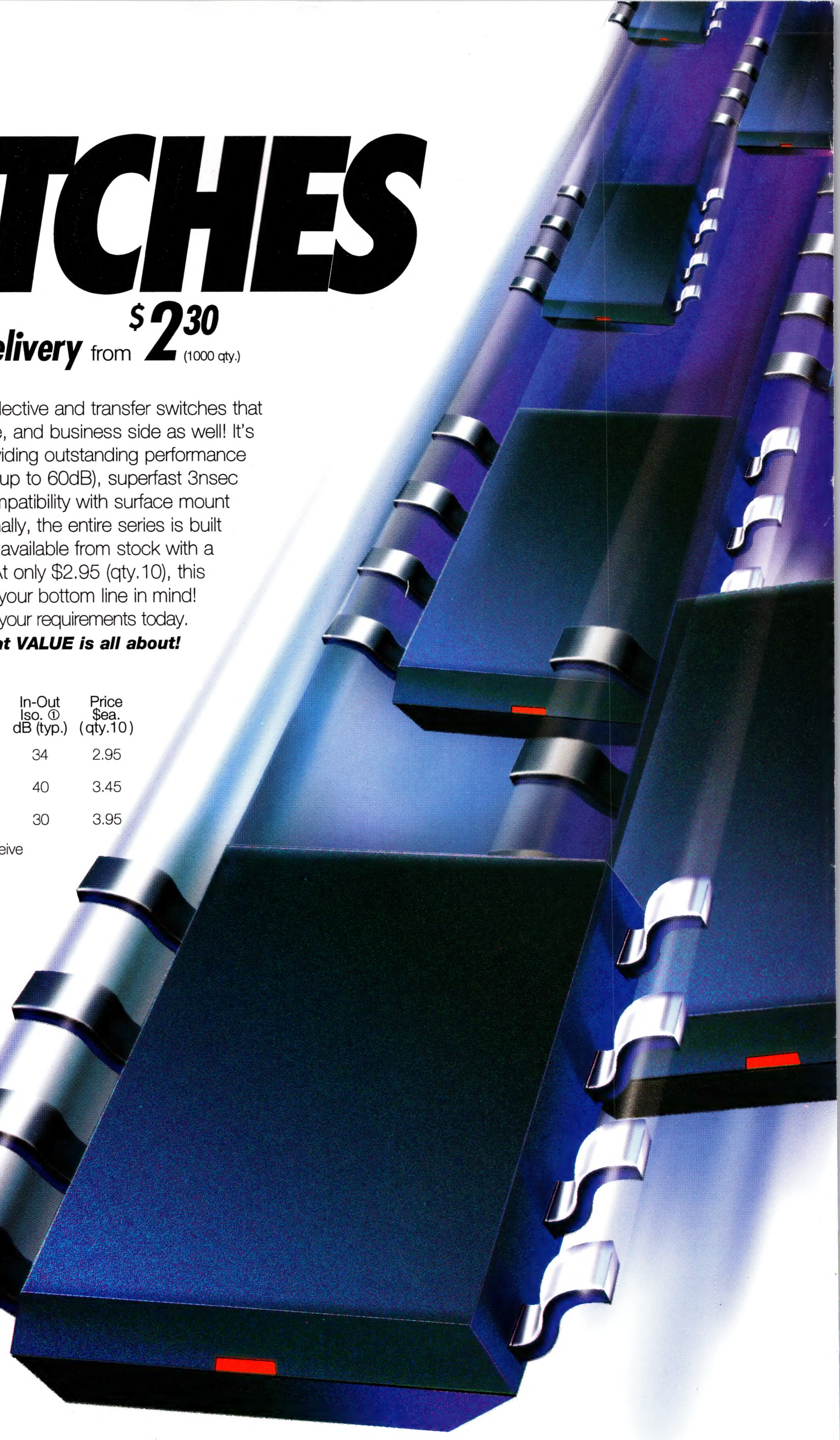

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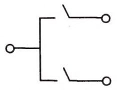

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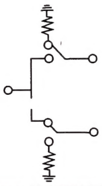

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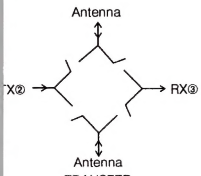

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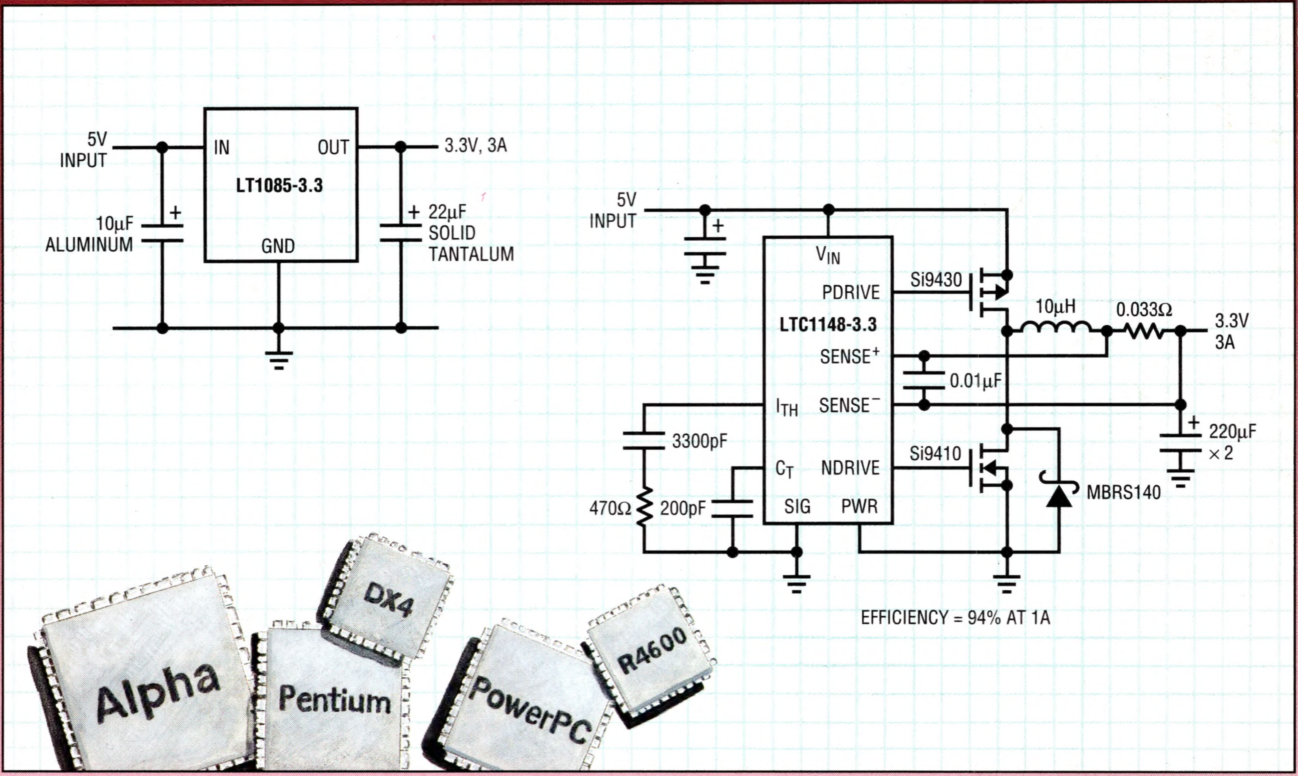

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Output Current	**Linear Regulator**	**Switching Regulator**
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3A	**LT1085-3.3**	**LTC1148-3.3**
5A	**LT1084-3.3**	**LTC1148-3.3**
7.5A	**LT1083**	**LTC1148-3.3**
10A	**LT1087 (X2)**	**LT1158**
15A (20A Peak)	**N/A**	**LT1158**

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